LASER XT SERIES

PERSONAL COMPUTER

Technical Reference Manual

VTECH

LASER XT SERIES

PERSONAL COMPUTER

Technical Reference Manual

For LASER TURBO XT,
LASER TURBO XT/2,
LASER TURBO XT/3

(The following is applicable to U.S.A. FCC class B version only)

This equipment generates and uses radio frequency energy. If it is not installed and used properly, that is, in strict accordance with the manufacturer's instructions, it may cause interference to radio and television reception.
It has been tested and found to comply with the limits for a Class B computing device in accordance with the specifications in Subpart J, Part 15, of FCC Rules. These rules are designed to provide reasonable protection against such interference in a residential installation. However, there is no guarantee that interference will not occur in a particular installation.
If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient the receiving antenna
- Relocate the computer with respect to the receiver
- Move the computer away from the receiver
- Plug the computer into a different outlet so that computer and receiver are on different branch circuits

If necessary, you should consult the dealer or an experienced radio/ television technician for additional suggestions. You may find the following booklet prepared by the Federal Communications Commission helpful: "How to Identify and Resolve Radio-TV Interference Problems"
This booklet is available from the U.S. Government Printing Office, Washington, DC20402, Stock No. 004-000-00345-4.

To ensure that the use of this product does not contribute to interference, it is necessary to use shielded I/O cables.

CAUTION :
Under no circumstances is this case to be opened.
This unit is not user-serviceable.

ATTENTION !
IL est interdit, Sous Aucun Pretexte D'ouvrir cette trousse. Cette Unite n'est pas utilisable A l'usager.

Copyright

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CHAPTER 1

OVERVIEW

1. Overview

1.1 Assembly of the computer

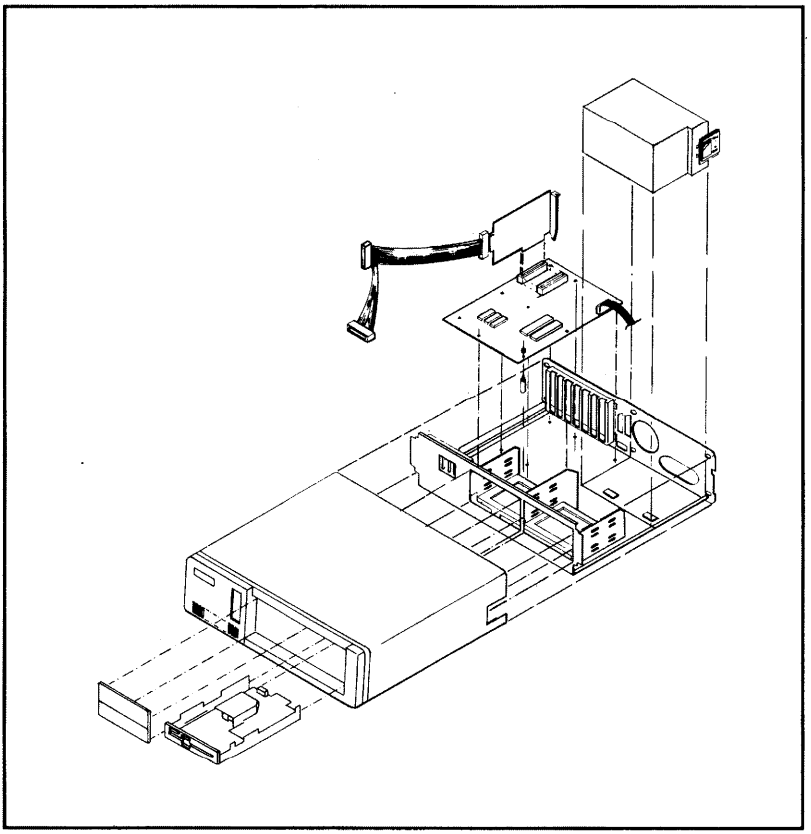


Fig 1.1 Exploded view of the Turbo XT and Turbo XT/2

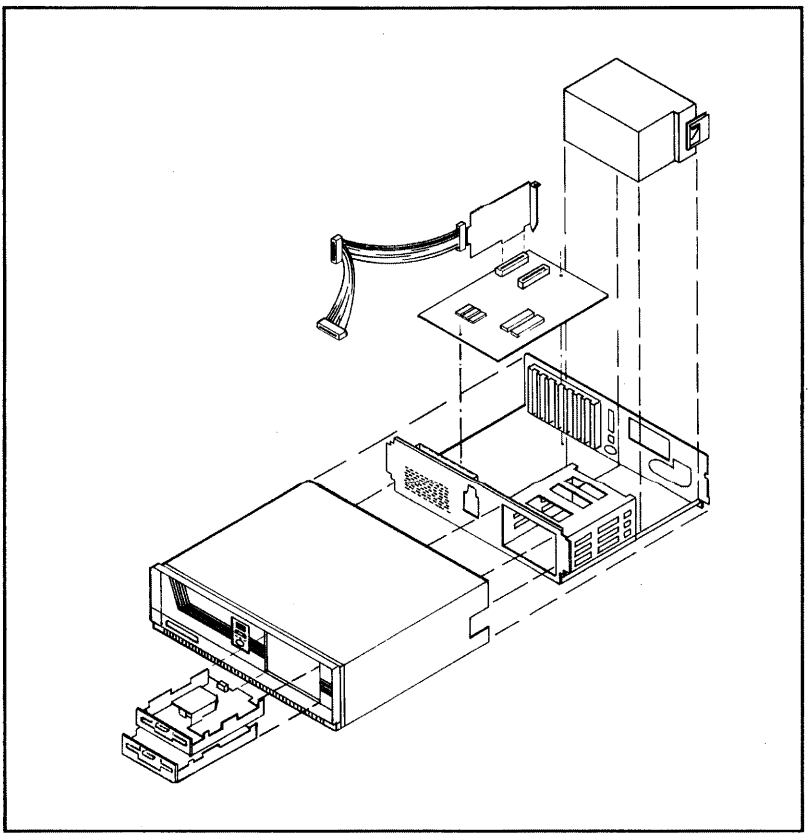


Fig 1.2 Exploded view of Turbo XT/3

1.2 System Board Diagram

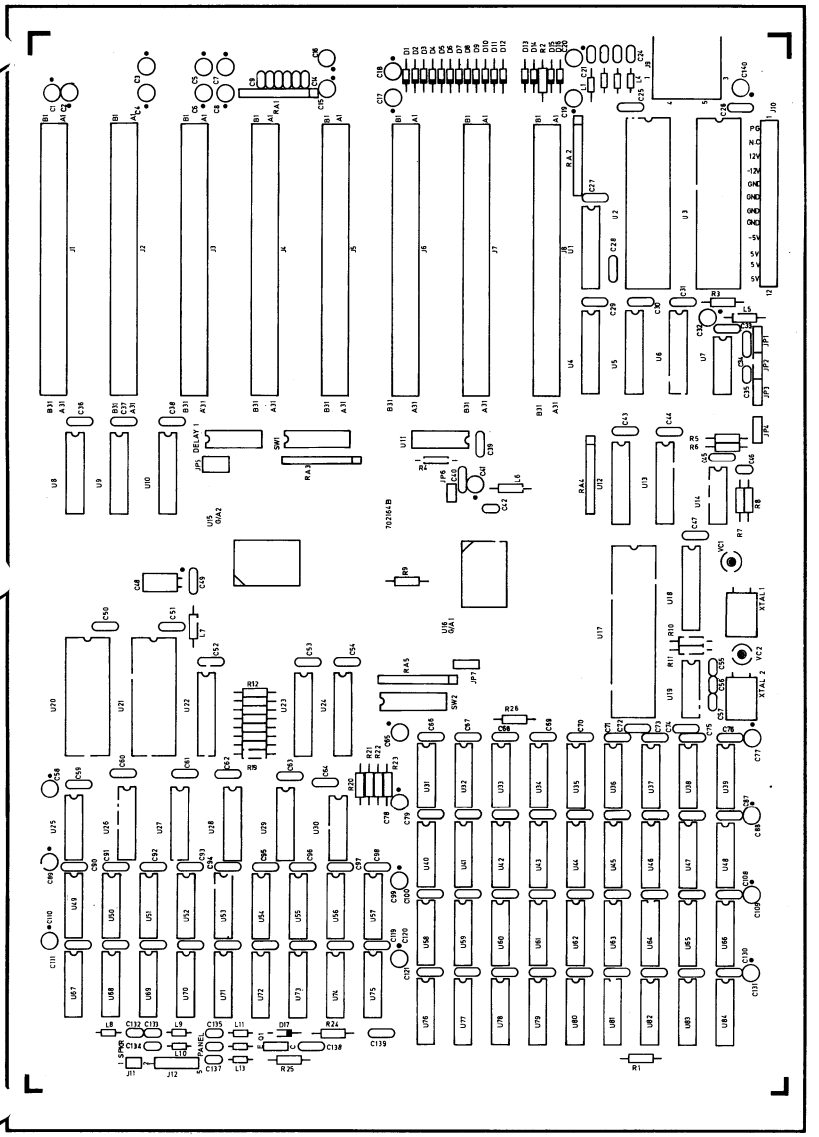


Fig 1.3 System board diagram of Turbo XT

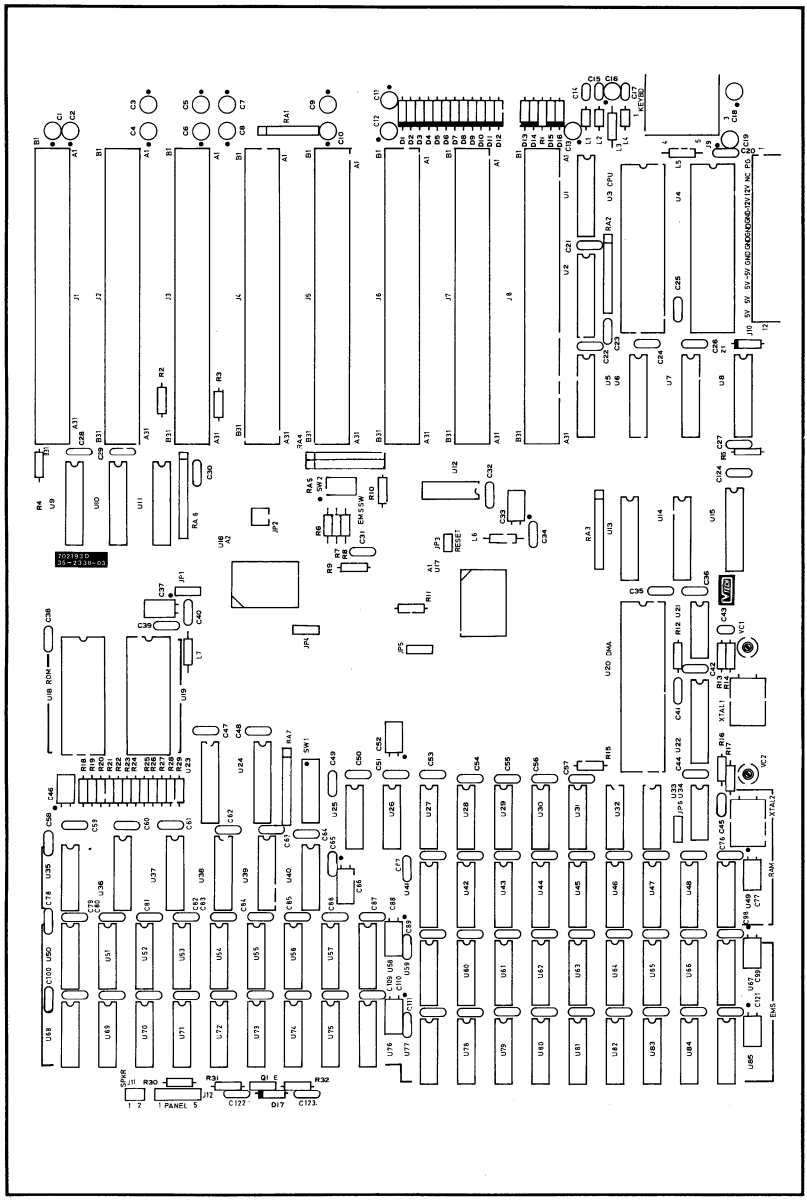


Fig 1.4 System board diagram of Turbo XT/2 and Turbo XT/3

1.3 Power Supply

The system DC power supply is a switching regulator. It operates at 130 watts or 150 watts. The DC voltages and DC currents supplied by power supply in various cases are listed in the following table:

Turbo XT	:	15A at +5V
or Turbo XT/2	:	4.2A at +12V
		0.3A at -5V
		0.3A at -12V
Turbo XT/3	:	15A at +5V
		5.2A at +12V
		0.3A at -5V
		0.3A at -12V

If DC over-load or over-voltage conditions exist, the supply with automatically be shut down. The AC input is also fused.

1.4 Keyboard

The keyboard layout resembles an ordinary typewriter. There are two types of keyboards offered to the users. One has 84 keys and the other is the XT enhanced keyboard with 101/102 keys. Most of the keys share the same functions. These two types of keyboards are detachable and interface to the main units via a 5 pin DIN type connector through a spiral cable.

1.5 Disk Drive

Turbo XT, XT/2 and XT/3 can accommodate two double-sided and double-density disk drives. They can be either 5 1/4" or 3 1/2" drive. Each 5 1/4" double-sided double-density floppy disk has a capacity of 360K bytes and has 40 tracks (track number ranges from 0 to 39). For the 3 1/2" floppy disk drive, the capacity is 720Kbytes and total no. of tracks is 80 (track no. ranges from 0 to 79). In some models, a hard disk may be installed. There are sufficient space within either Turbo XT,XT/2 or XT/3.

The number of floppy disk drives installed should be set by setting the DIP switch DIP-SW1 properly according to the following diagram.

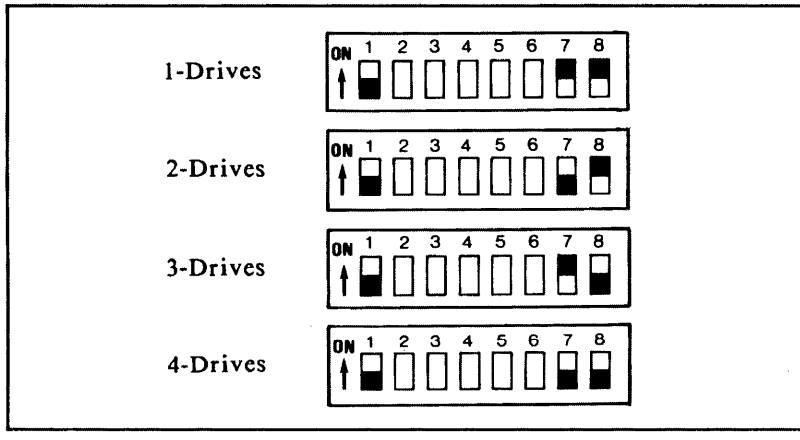


Fig 1.5 DIP switch settings for disk drives

1.6 Front Panel

1.6.1 Front Panel of Turbo XT and Turbo XT/2

On the front panel there is a keyboard lock. When the lock is on, all characters typed on the keyboard will be ignored.

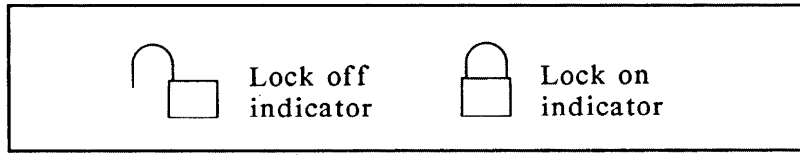


Fig 1.6 Keyboard Lock Indicator

There are also a power indicator and a high speed indicator. When the LED of the high speed indicator is lit, the CPU is running at high speed mode.

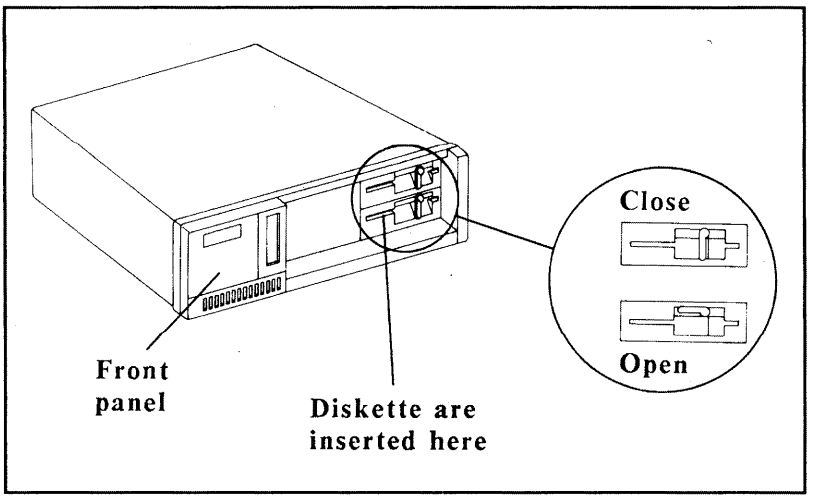


Fig 1.7 Front Panel of Turbo XT or Turbo XT/2

1.6.2 Front panel of Turbo XT/3

On the front panel, there is a keyboard and reset security lock. The positions and corresponding functions of the lock is listed as below:-

Position	Keyboard	Reset button
Left Right	Unlock lock	enable disable

The reset button on the front panel is used for hardware reset of the system.

Located at top of the front panel is a dual - seven-segment LED. A "5" will be displayed when the CPU operates at 4.77MHz and a "10" will be displayed when CPU operates at 10MHz.

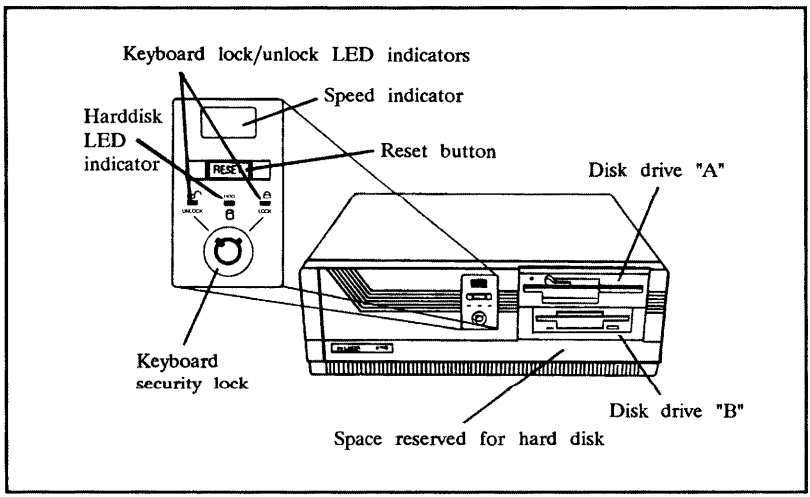


Fig 1.8 Front Panel of Turbo XT/3
(showing 5-1/4" Drive and 3-1/2" Drive)

Some versions of the Turbo XT/3 may have a different front panel. It differs from that described above by having one more LED indicator in between the lock and unlock LED indicators. It can be used to indicate hard disk drive access if the system has a hard disk installed and the hard disk controller had the appropriate signal.

CHAPTER 2

SYSTEM BOARD

2. SYSTEM BOARD

2.1 Block Diagram

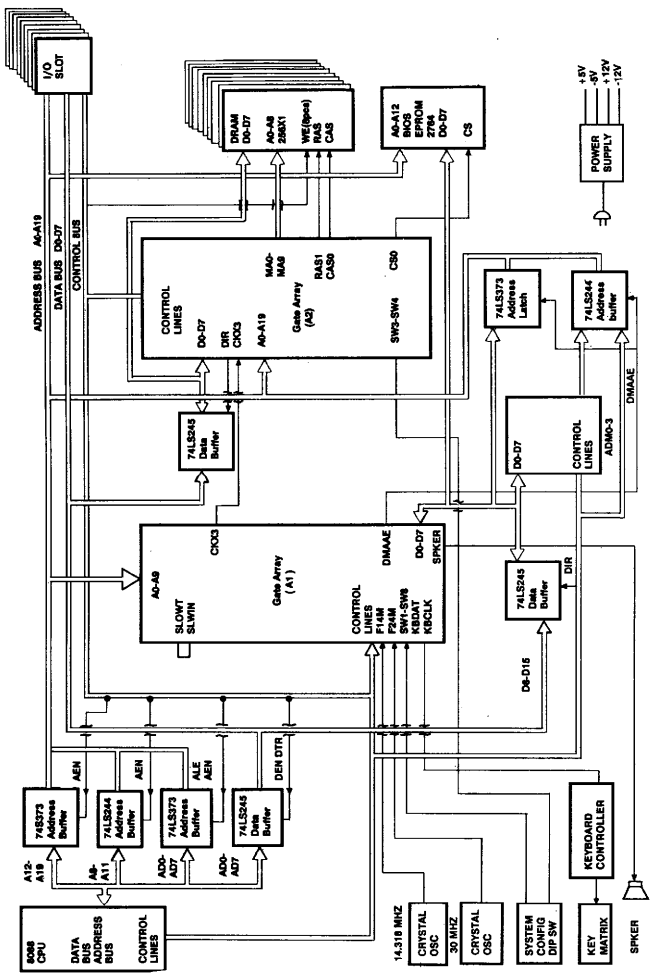


Fig 2.1 System board block diagram of Turbo XT

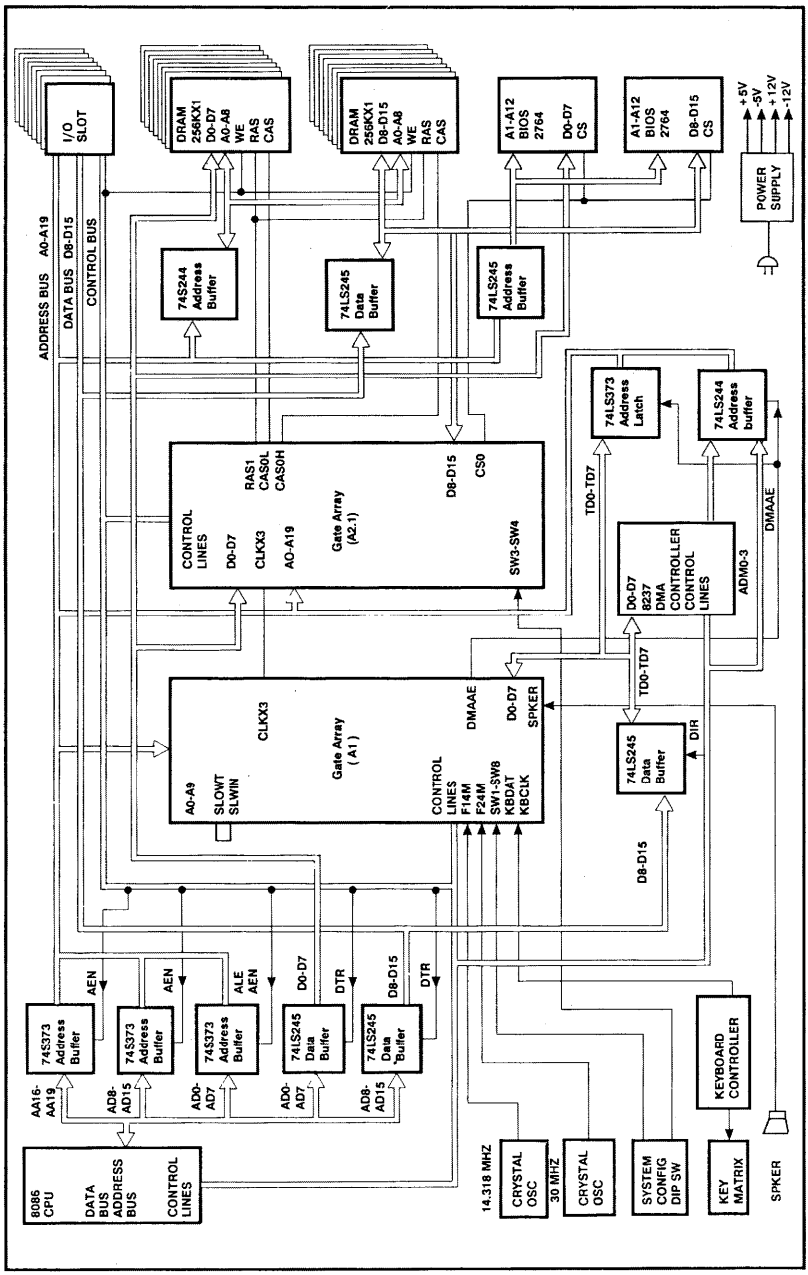


Fig 2.2 system board block diagram of Turbo XT/2 and Turbo XT/3

2.2 Microprocessor

The CPU of Laser Turbo XT is the Intel 8088-1 (or 8088-2 in the 8MHZ model), while both Turbo XT/2 and Turbo XT/3 use Intel 8086-1 as the CPU. Both 8088 and 8086 are high performance microprocessor implemented in N-channel, depletion load, silicon gate technology (HMOS), and packaged in a 40-pin DIP package.

The CPU 8088-1 have the following features:

- 8-bit data bus interface for 8088-1, 16-bit data bus interface for 8086-1.
- 16-bit internal architecture
- Direct addressing capability to 1 Mbyte of memory
- Direct software compatibility between 8086 and 8088
- 14-word by 16-bit register set with symmetrical operations
- 24 operand addressing modes
- Byte, word and block operations
- 8-bit and 16-bit signed and unsigned arithmetic in binary or decimal, including multiply and divide.
- Clock rate of 10 MHZ.

Remark: i) 8086 is almost identical with 8088, with the exception that 8088 handles only 8-bit data bus while 8086 handles 16-bit data bus.The result is that 8088 takes a longer execution time than 8086. Also, the pin outs for 8088 and 8086 are ass different.

ii) 8088, 8086 operates at 5MHz, 8088-1, 8086-1 operates at 10MHz, 8088-2, 8086-2 operates at 8MHz.

On the Turbo XT, XT/2 and XT/3, the CPU can be driven at two clock speed - 4.77MHz and 10 MHz. At 4.77MHz, memory accesses take four clock cycles (840ns). While I/O accesses take five clock cycles (1050ns). At 10 MHz, the internal RAM accesses take four cycles (400ns). I/O accesses still take 5 cycles. However, the clock is slowed down to 4.77MHz for all I/O accesses. The same is true for DMA cycles. This ensure the Turbo XT is compatible with most expansion cards when running even at 10 MHz which is more than twice the normal speed.

2.3 Coprocessor

An 8087 numeric data coprocessor can be installed to provide instructions and data types needed for high performance numeric applications.

The 8087 is a numeric processor extension that performs arithmetic and logical instruction on many types of numeric data. It also executes many built-in transcendental functions. The 8087 is treated as an extension to the CPU, providing register, data types, control, and instruction capabilities at the hardware level. The programmers can treat the CPU and the 8087 as a single processor.

The 8087 is offered in three versions:

- the 8087 (5MHz)
  8087-2 (8MHz)
  8087-1 (10MHz)

The 8088-1 must be used if the computer is to be operated at 10 MHz.

2.4 RAM (Random - Access Memory)

If your computer is Turbo XT, please refer to fig. 2.3; refer to fig. 2.4 otherwise. In any case, the computer have 640K of conventional RAM on board located at row 1 to row 4. Row 5 to Row 8 are 4 rows of sockets for the expanded memory.

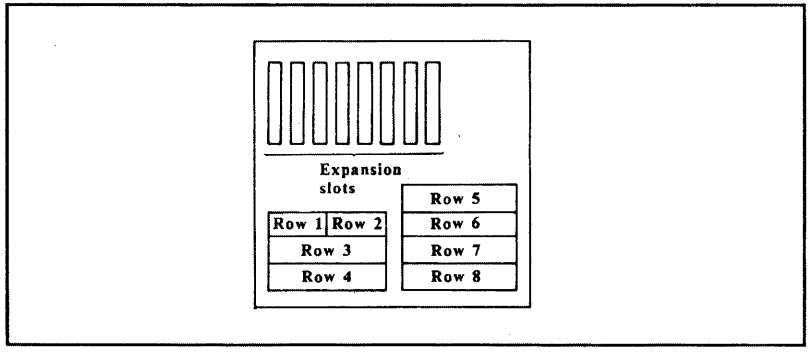


Fig 2.3 Layout of RAM on PCB of Turbo XT

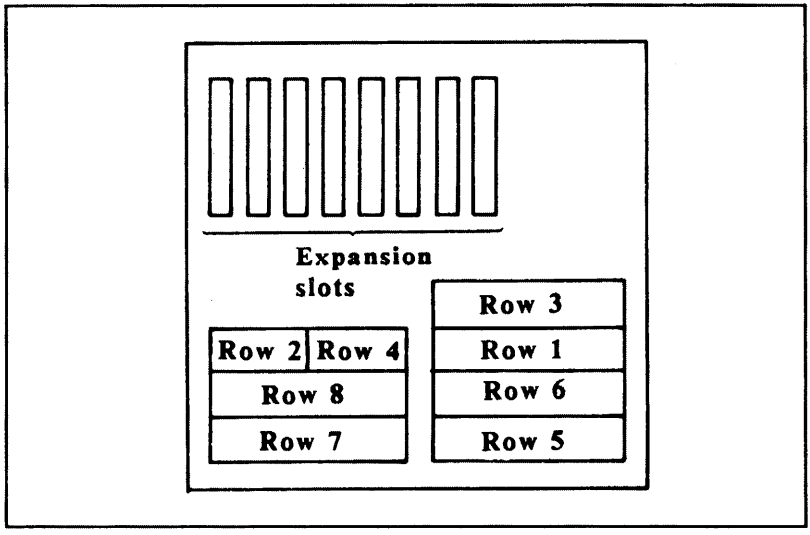


Fig 2.4 Layout of RAM on PCB of Turbo XT/2 and Turbo XT/3

Row 1 and Row 2 both make up of two 4464 and one 4164, Row 3 and Row 4 are two row of 41256, these four rows of RAM make up totally 640K of memory on board. These portion of RAM that the DOS can recognize is known as conventional memory. For the amount of conventional memory installed on board of Turbo XT the DIP switch SW1 should be set properly according to the following diagram.

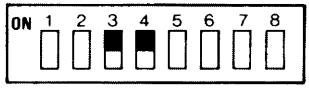
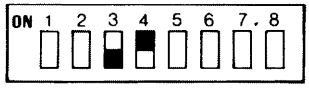
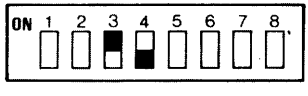
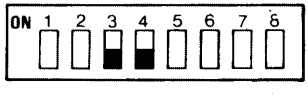
Amount of Conventional Memory	System DIP Switch	Bank Enabled
256K		0
512K		0, 1
576K		0, 1, 2
640K		0, 1, 2, 3

Fig 2.5 DIP switch SW1 settings for memory installed

Row 5 to Row 8 are four row of sockets for expanded memory. They should be inserted with 41256 and start inserting from Row 5. When all sockets are inserted with 41256, the total expanded memory will be 1Mbyte.

For Turbo XT/2 and Turbo XT/3, POLE 4 of SW1 is not used, while POLE 3 OFF indicates 512K RAM on board and POLE 3 ON indicates 640K.

For the amount of expanded memory installed, the DIP switch SW2 should be set properly. If your computer is Turbo XT, then refer to Fig. 2.6 You may imagine that there are two expanded memory cards installed on the mainboard. The first consists of Row 5 and Row 6. The other consists of Row 7 and Row 8. Each card has a set of I/O ports for control purposes. The addresses of these I/O ports must be unique for each card. A 8 pole DIP switch is used to set these addresses.

If your computer is Turbo XT/2 or Turbo XT/3, then refer to fig 2.7 You may imagine that there is one expanded memory card on mainboard in this case.

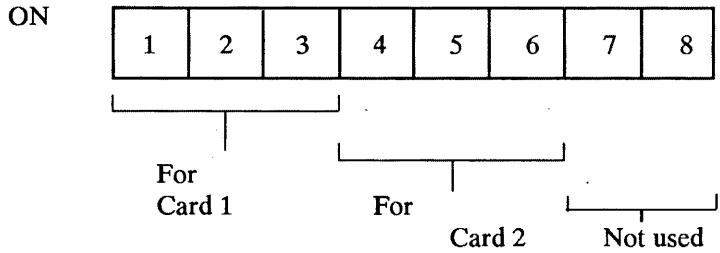


Fig. 2.6: DIP switch SW2 in Turbo XT.

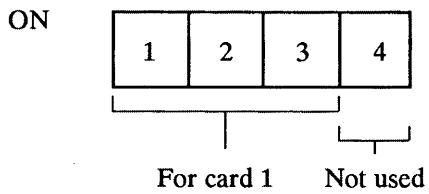
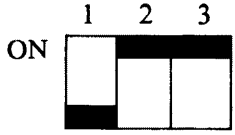
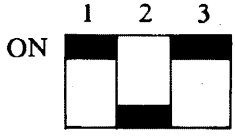


Fig 2.7: DIP switch SW2 in Turbo XT/2 or Turbo XT/3

DIP switch setting I/O port address (in Hex)



208



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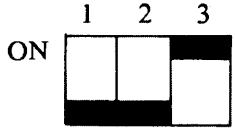

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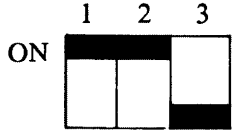

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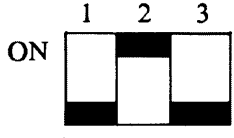
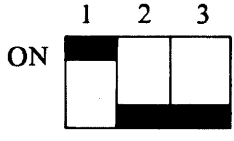


2A8



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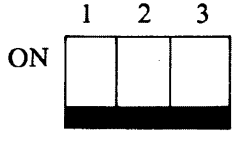

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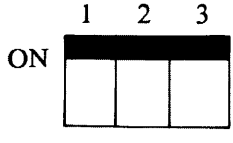
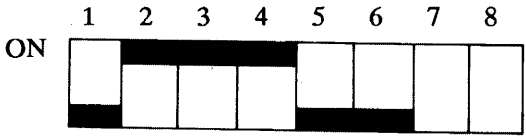


Disable the on board expanded memory

For example, in Turbo XT the following DIP-switch setting configures card 1 at address 208H and card 2 at 2B8H.

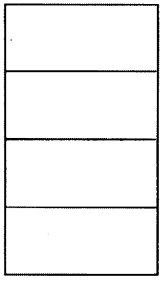


The access time of the DRAM chips has to be 150ns or less for 8MHz high speed operation. For the 10MHz model 120ns DRAM is required.

2.5 ROM (Read Only Memory)

In Turbo XT, there are two 28-pin sockets for ROM, one of them is occupied by a 2764 which stored the BIOS (Basic Input Output System). The other empty socket is used to house a 32K ROM, such as the BASIC ROM.

The contents of the BASIC ROM should be arranged as follows.



map to physical addresses F6000H-F7FFFH

map to physical addresses FC000H-FDFFFH

map to physical addresses FA000H-FBFFFH

map to physical addresses F8000H-F9FFFH

In Turbo XT/2 and Turbo XT/3, there are two 28-pin sockets for ROM, both of them are occupied by 2764 which stored the BIOS. The contents of the two 2764 are identical. One of them contribute the ODD Byte to the system and the other EVEN Byte. Together they support 16 Bit BIOS access.

2.6 Interrupt Subsystem

There are eight prioritized levels of interrupt, six are available on the system expansion slots for use by expansion cards. Two levels are used on the system board. Level 0 is connected to channel 0 of the timer to provide a periodic interrupt for the time-of-day clock.

Level 1 is used by the keyboard interface. Whenever a scan code from the keyboard is received an interrupt will be initiated.

The non-maskable interrupt (NMI) of the CPU is connected to the memory parity checking circuitry. It is also used by the 8087 coprocessor to report errors. Fig 2.8 is the listing of the system interrupt.

Number	Usage
NMI	Parity 8087
0	Timer
1	Keyboard
2	EGA
3	RS232 COM2
4	RS232 COM1
5	Hard disk
6	Diskette
7	Printer

Fig 2.8 Hardware interrupt listing

The interrupt controller and NMI circuitry are integrated into the gate array A1.

2.7 DMA (Direct Memory Access)

The Turbo XT, Turbo XT/2 and XT/3 all employ a 8237A-5 Direct Memory Access (DMA) controller to perform the DMA function.

The 8237A-5 contains 344 bits of internal memory in the form of registers. Fig 2-9 is the listing of these registers.

Name	Size (bit)	No.
Base Address Registers	16	4
Base Word Count Registers	16	4
Current Address Registers	16	4
Current Word Count Registers	16	4
Temporary Address Register	16	1
Temporary Word Count Register	16	1
Status Register	8	1
Command Register	8	1
Temporary Register	8	1
Mode Registers	6	4
Mask Register	4	1
Request Register	4	1

Fig 2.9 8237A-5 internal registers

The 8237 only provides 16 bits of address A0-A15. An additional DMA page register is used to provide the highest 4 bits of addresses A16-A19 so that the entire 1M address space can be accessed. The DMA page register is located at gate array A2 or A2.1.

The following figure shows the addresses of the DMA page register.

I/O address	R/W	Register
81H	W	Page register for DMA channel 2
82H	W	Page register for DMA channel 3
83H	W	Page register for DMA channel 1

Fig 2.10 DMA page register.

The DMA channel 0 is normally reserved for the function of dynamic RAM refreshing.

2.8 Timer

The Programmable Interval Timer is integrated in the gate array A1 and have the register set shown below.

I/O address	R/W	Register
40H	R/W	Counter 0
41H	R/W	Counter 1
42H	R/W	Counter 2
43H	W	Counter Word

Fig 2.11 Programmable interval timer register set.

Counter 0 is used as a general purpose timer. Counter 1 is used to count and request refresh cycles. Counter 2 is used as a tone generation for the loudspeaker. All timer are clocked at 1.19MHz.

2.9 CPU Speed Control Port

The CPU speed control port is a R/W register with address 1F0H. The first seven bits of the register is not used. Bit 7 is used to set the speed mode of the computer. When its content is 0, the CPU is running at standard speed (4.77MHz). When its content is 1, the CPU is running at high speed mode.

2.10 Expanded Memory

The gate array A2 or gate array A2.1 in 8088 MODE can supports three Expanded Memory Boards (Only two are used on the Turbo XT) with each one contains a maximum of 2 Mbyte RAM. For A2.1 in 8086 mode, one expanded memory board is supported 1 Mbit DRAM can be supported while 41256 can also be used. On the TURBO XT, Turbo XT/2 or Turbo XT/3, four Row of 41256 are used to provide a total of 1Mbytes of Expanded Memory.

Each Expanded Memory Board is controlled via eight I/O ports. The addresses of these ports are determined by external DIP switches settings. For A2 or A2.1 in 8088 mode, ESWO-ESW2 determine address of board 0 while ESW3-ESW5 for board 1 and ESW6-ESW8 for board 2. (ESW6-ESW8 are shorted to ground on the Turbo XT). For A2.1 in 8086 mode, ESW0-ESW2 betermine address of the only board.

Fig2.12 Summarizes the DIP switches settings and the corresponding Page Mapping Register and Control Register for the Expanded Memory Board.

ESW2 ESW5 ESW8	ESW1 ESW4 ESW7	ESW0 ESW3 ESW6	Page Mapping Register	Control Register
			Expanded memory disabled	
0	0	0		
0	1	0	208H, 4208H, 8208H, C208H	0209H, 4209H,8209H, C209H
0	1	0	0218H, 4218H, 8218H, C218H	0219H, 4219H, 8219H, C219H
0	1	1	0258H, 4258H,8258H,C258H	0259H, 4259H, 8259H,C259H
1	0	0	0268H, 4268H, 8268H, C268H	0269H, 4269H, 8269H,C269H
1	0	1	02A8H,42A8H, 82A8H, C2A8H	02A9H,42A9H, 82A9H, C2A9
1	1	0	02B8H, 42B8H, 82B8H,C2B8H	02B9H, 42B9H, 82B9H,C2B9H
1	1	1	02E8H, 42E8H, 82E8H, C2E8H	02E9H, 42E9H,82E9H, C2E9H

Fig2.12 The relation between DIP switches settings and the corresponding Page Mapping Register and Control Register for the Expanded Memory Board.

The expanded memory occupy 64K of contiguous memory space. The starting address is determined by the Control Register. Fig 2.13 shows the relation between bit 7 of the control Registers and the starting address.

Bit 7 of 82 x 9H	Bit 7 of 42 x 9H	Bit 7 of 02 x 9H	Starting address
0	0	0	C4000H
0	0	1	C8000H
0	1	0	CC000H
1	1	1	D0000H
1	0	0	D4000H
1	0	1	D8000H
1	1	0	DC000H
1	1	1	E0000H

X=0, 1, 5, 6, A, B, E

Fig 2.13 relation between control resisters and starting address.

Bit 7 of C2X9 are not used.

The Expanded Memory is accessed in 16K page. There are four Page Mapping Registers used to enabling, disabling, and swapping the various pages in and out of the system memory space. Each board can support up to 128 pages, thus using 7 of these 8 bits in each Page Mapping Register. The eighth bit is a page enable/disable bit when set (1 or high), it allows the page to appear in the memory space. When clear (0 or low), the page does not appear in the memory space. This enabling/disabling is necessary to avoid read conflicts between different boards in the system. Fig 2.14 shows the relation between the Page Mapping Register and the corresponding 16K memory window.

I/O address	R/W	16K window
02X8H	R/W	Y0000-Y3FFFH
42X8H	R/W	Y4000-Y7FFFH
82X8H	R/W	Y8000-YBFFFH
C2X8H	R/W	YC000-YFFFFH

X=0,1,5,6,A,B,E
Y is a don't care

Fig 2.14 Relation between Page Mapping Register and the corresponding 16K memory Window

For example, if the Expanded Memory starts from address C4000H, then the port 02X8H controls the D000H-D3FFFH window, 42X8H controls the C4000H-C7FFFH window, 82X8H controls the C8000-CBFFFH window and C2X8H controls the CC000H-CFFFFH window.

On the TURBO XT, the expanded memory pages are partially decoded. For example, page number 80H and 90H will reference the same page. The details are as follow

RAM Location	Descriptions	
Row 5	Board 0	Page C0H-CFH Partially decoded through C0H-FFH
Row 6	Board 0	Page 80H-8FH Partially decoded through 80H-BFH
Row 7	Board 1	Page C0H-CFH Partially decoded through C0H-FFH
Row 8	Board 1	Page 80-8FH Partially decoded through 80-BFH

On Turbo XT/2 and Turbo XT/3, however, the expanded memory pages are not partially decoded.

2.11 Speaker

The sound system has a small speaker. The speaker can be driven from one or both of two sources:

. By setting & resetting BIT 1 of I/O port 61H.

. By timer channel, this timer is clocked by a 1.19 MHz clock. The timer gate is also controlled by bit 0 of I/O port 61H.

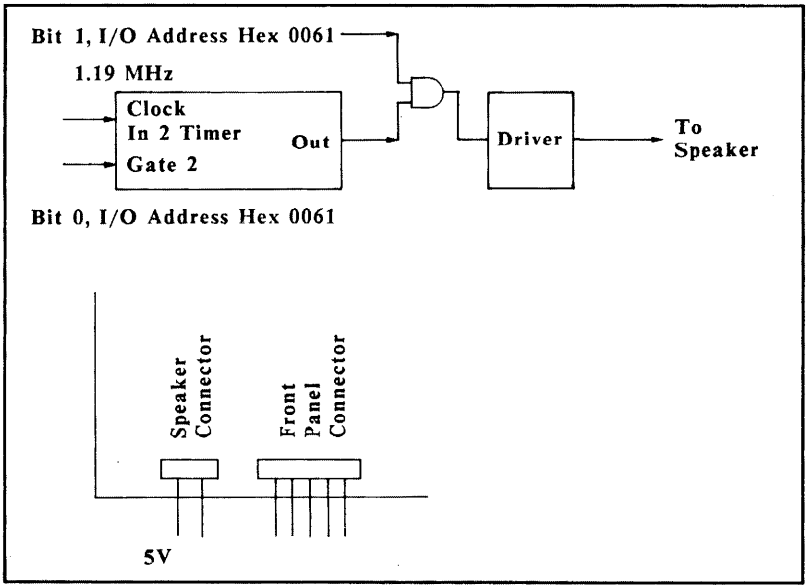


Fig 2.15 Speaker connector.

2.12 Front panel connector

A five pin jumper J12 is situated at the right bottom of the PCB, the pin 1 and pin 2 of the front panel connector are for keyboard lock, if these two pins are opened, any data entered from the keyboard will not be recognized.

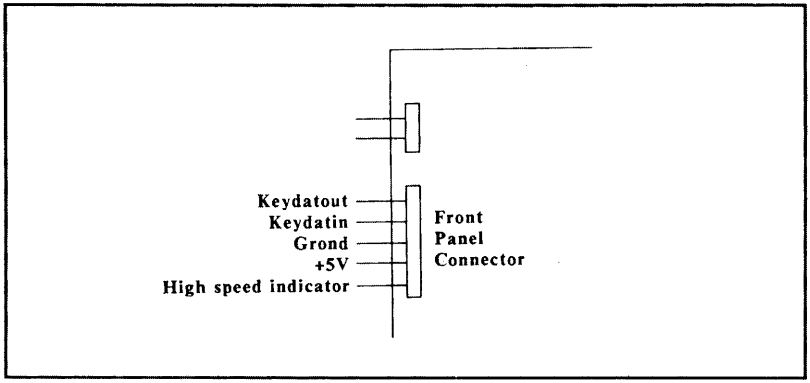


Fig 2.16 Front panel connector

2.13 Memory Map

Start Address Decimal	Hex	Function
0	00000	
16K	04000	
32K	08000	
48K	0C000	
64K	10000	
80K	14000	
96K	18000	
112K	1C000	
128K	20000	
144K	24000	
160K	28000	
176K	2C000	
192K	30000	
208K	34000	
224K	38000	
240K	3C000	

Start Address Decimal	Start Address Hex	Function
256K	40000	256-640K Read/Write Memory on System Board
272K	44000	
288K	48000	
304K	4C000	
320K	50000	
336K	54000	
352K	58000	
368K	5C000	
384K	60000	
400K	64000	
416K	68000	
432K	6C000	
448K	70000	
464K	74000	
480K	78000	
496K	7C000	
512K	80000	
528K	84000	
544K	88000	
560K	8C000	
576K	90000	
592K	94000	
608K	98000	
624K	9C000	
640K	A0000	128K Reserved
656K	A4000	
672K	A8000	
688K	AC000	

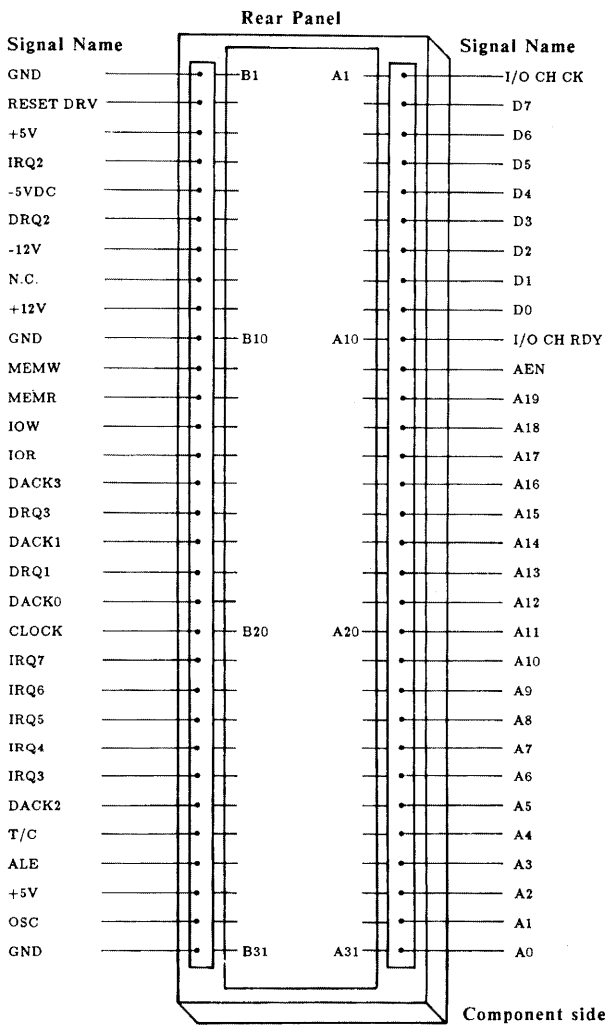
Start Address Decimal	Hex	Function
704K	B0000	Monochrome
720K	B4000	
736K	B8000	Color/Graphics
752K	BC000	
768K	C0000	EGA BIOS
784K	C4000	
800K	C8000	Fixed Disk Control
816K	CC000	
832K	D0000	
848K	D4000	192K Read only
864K	D8000	Memory
880K	DC000	Expansion and
896K	E0000	Control
912K	E4000	
928K	E8000	
944K	EC000	
960K	F0000	
976K	F4000	64K Base System
992K	F8000	ROM
1008K	FC000	BIOS AND BASIC

2.14 I/O MAP

Hex Range	Usage
000-00F	DMA Chip 8237A-5
020-021	Interrupt controller
040-043	Timer
060-063	PPI
080-083	DMA Page Registers
0A0	NMI Mask Register
200-20F	Game Control
210-217	Expansion Unit
2F8-2FF	Asynchronious Communications (Secondary)
300-31F	Prototype Card
320-32F	Fixed Disk
378-37F	Parallel Printer
380-38F	SDLC Communications
3B0-3BF	Monochrome Display Printer
3D0-3DF	Color/Graphics
3F0-3F7	Diskette
3F8-3FF	Asynchronious Communications (Primary)

2.15 I/O Slots

2.15.1 I/O channel diagram



2.15.2 I/O channel signal description

The following is a description of the I/O channel signal. All lines are TTL-compatible.

Signal	I/O	Description
OSC	O	Oscillator : 14.31818 MHz clock. It has a 50% duty cycle.
CLOCK	O	System Clock : It is the CPU clock, it has a period of 210 ns (4.77MHz) in normal mode and a period of 100ns (10MHz) in high speed mode. The clock has a 33% duty cycle.
RESET DRV	O	This line is used to reset system logic on power up or when the line voltage is too low. This signal is synchronized to the falling edge of clock and is active high.
A0-A19	O	Address Bits 0 to 19: These lines are used to address memory and I/O devices within the system. The 20 address lines allow access of up to 1 megabyte of memory. These lines are generated by either the processor or DMA controller.
D0-D7	I/O	Data Bits 0 to 7: These lines provide data bus bits 0 to 7 for the processor, memory, and I/O devices.

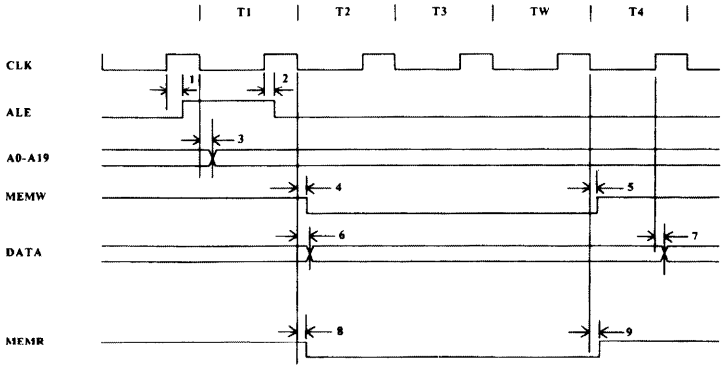
Signal	I/O	Description
ALE	O	Address Latch Enable: This line is driven by the bus controller and is used to latch valid addresses from the processor. Processor addresses are latched with the falling edge of ALE.
I/O CH CK	I	I/O Channel Check: When this signal is active low, a parity error is indicated and the NMI signal to the processor will be activated.
I/O CH RDY	I	I/O Channel Ready: This line, normally high (ready), is pulled low (not ready) by a memory or I/O device to insert wait states. It allows slower devices to attach to the I/O channel. This line should be asserted immediately when a valid address and the read write command are detected. This line cannot be held longer than 10 clock cycles.
IRQ2-IRQ7	I	Interrupt Request 2 to 7: These lines are used to request services from the processor. IRQ 2 has the highest priority and IRQ7 has the lowest. An interrupt request is generated by asserting an IRQ line (low to high) and holding it high until it is acknowledged by the processor (interrupt service routine).
IOR	O	-I/O Read Command: This command is used to read data from an I/O device. It may be driven by the processor or the DMA controller. This signal is active low.

Signal	I/O	Description
IOW	O	-I/O Write Command: This command is used to strobe data into an I/O device. It may be driven by the processor or the DMA controller. This signal is active low.
MEMR	O	Memory Read Command: This command line is used to read a memory. It may be driven by the processor or the DMA controller. This signal is active low.
MEMW	O	Memory Write Command: This command line is used to strobe data into a memory. It may be driven by the processor or the DMA controller, this signal is active low.
DRQ1-DRQ3	I	DMA Request 1 to 3: These lines are used to request DMA service, DRQ 3 has the lowest priority and DRQ1 has the highest. A request is generated by asserting a DRQ line to high. A DRQ line must be held high until the corresponding BACK line goes active.
BACK0-BACK3	O	-DMA Acknowledge 0 to 3: These lines are used to acknowledge DMA requests (DRQ1-DRQ3). They are active low. Back0 is used to refresh dynamic RAM.
AEN	O	Address Enable: When this signal is high, the address bus, data bus and read-write command lines are driven by the DMA controller.
T/C	O	Terminal Count: When the terminal count for any DMA channel is reached, a pulse will be output on this line. This signal is active high.

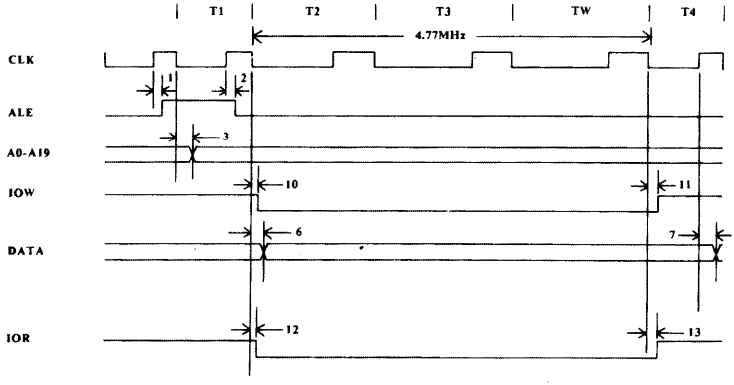
2.15.3 I/O SLOT TIMING at high speed

(Vcc = 5V +/-5%, Ta = 0 To 70 C)

		Min (ns)	Type (ns)	Max (ns)
1.	ALE active delay from CLK	17		84
2.	ALE inactive delay from CLK	2		15
3.	A0-A19 delay from CLK			72
4.	MEMW active delay	4	12	25
5.	MEMW inactive delay	2	8	17
6.	D0-D7 (write) delay			71
7.	D0-D7 (write) delay			58
8.	MEMR active delay	4	12	25
9.	MEMR inactive delay	2	8	17
10.	LOW active delay	4	12	25
11.	LOW inactive delay	2	8	17
12.	IOR active delay	4	12	25
13.	IOR inactive delay	2	8	17



MEMR AND MEMW TIMING AT HIGH SPEED MODE



IOR AND IOW AT HIGH SPEED MODE

CHAPTER 3

KEYBOARD

3. KEYBOARD

3.1 Keyboard Layout

There are various types of keyboards offered to the users. One is the XT enhanced keyboard with 101/102 keys.

To describe the keyboard clearly, it has been divided into three section according to their different functions.

1: Typewriter key and control keys
2: Numeric Keypad and edit keys
3: Function keys.

U.K. ENGLISH K102-3 ENHANCED LAYOUT

This Enhanced layout keyboard should be equipped with PC/AT or compatible or new PC/XT system and operating system must be PC DOS 3.2; 3.3 or newer version.

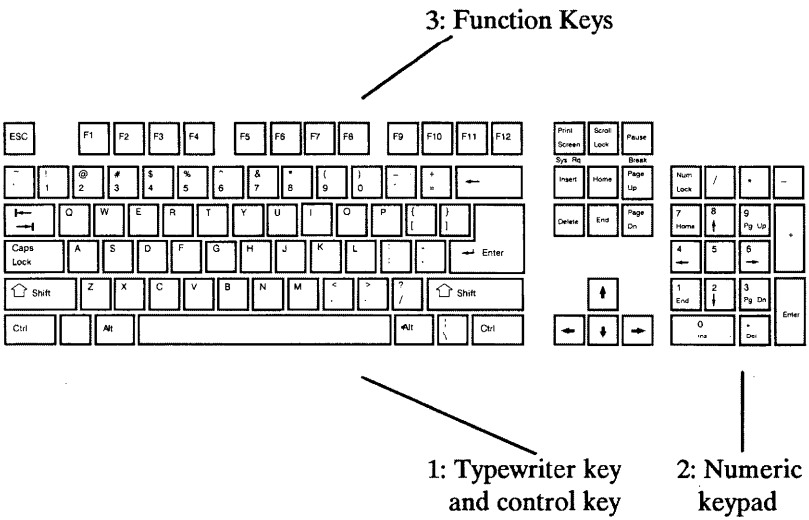


Fig 3.1 Layout of 102 keys keyboard.

3.2 Keyboard Connector

3.2.1 keyboard Connector Specification

The keyboard connector is a 5-pin DIN connector, its pin assignment is illustrated in Fig. 3.2

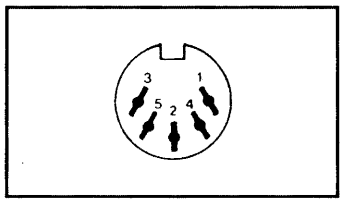


Fig 3.2 Pin assignment of the 5-pin DIN connector

The keyboard connector specification is as follow:

Pin	TTL Signal
1	+Keyboard Clock
2	+Keyboard data
3	-Keyboard Reset (Not Used)
4	Ground
5	+5 Volts

3.2.2 Keyboard Connector Signal Description

There are totally five signal lines connecting the keyboard controller to the computer mainboard.

They are :

(1)	KBDATA	-	Keyboard data
(2)	KBDCLK	-	Keyboard clock
(3)	KRES	-	Keyboard reset
(4)	GND	-	Signal ground
(5)	Vcc	-	+5V DC Supply.

KRES line is not used (N.C.) in the current circuit KBDATA line is a bi-directional line driven by open-collector devices. It is normally low when no signal is transferring.

KBDCLK line is a bi-directional line driven by open-collector devices. It is normally high when no signal is transferring.

3.3 SCAN CODES

3.3.1 Scan Codes Description

On the Laser Turbo XT Turbo XT/2 and Turbo XT/3, as the other IBM PC/XT compatible machines, the keyboard controller is responsible for generating "Scan code" instead of ASCII code. These Scan codes are arbitrary assigned and their meaning are interpreted by the system BIOS or the application programs running. This allows for easy modification to support foreign language keyboards.

Scan codes are classified as "Make" and "Break" codes. Make/Break codes of the same key only differs in the most significant bit (Bit 7). Make code has MSB = 0, while Break code has MSB = 1.

Not all possible scan code are recognized by the system BIOS. Some invalid scan codes are ignored by the system BIOS, and some forbidden scan code produces "beep" sound when the system BIOS detects it.

"Make" codes are generated when a key is depressed, i.e, changes from OFF state to ON state. If the key is depressed for a certain length of time (Say 1/2 second), the same "Make" code as above will be generated and transmitted to the main unit at a rate of approximately 10 times each second. This "autorepeating" feature is also known as "typematic".

All the keys on the conventional IBM® PC/XT keyboard are typematic, however, some keys on the Enhanced Keyboard are not typematic, i.e, make codes are generated when the key is pressed for the first time, but holding the key down will not generate any further make codes (e.g. Pause key in Enhanced Keyboard).

"Break" codes are generated when a key is released, i.e, changes from ON state to the OFF state.

The delay time before typematic occurs is approximately 1/2 second. Typematic rate is approximately 10 codes (code sequence in multi-code conditions) per second. That is, after you have pressed the key and hold down for 1/2 seconds, there will be 10 characters per second generated on the screen.

3.3.2 Scan Codes Details

Terminology used:

1.	CAPS LOCK ON	=	The CAPS LOCK LED IS ON. ie, the main unit interprets capital letter.
2.	CAPS LOCK OFF	=	The CAPS LOCK LED IS OFF. ie, the main unit interprets small case letter.
3.	Ctrl ON	=	The Ctrl key (either left or right) is already depressed and not yet released.
4.	Ctrl OFF	=	The Ctrl key is not depressed.
5.	SHIFT ON	=	The Shift key (either, left or right) is already depressed and not yet released.
6.	SHIFT OFF	=	The shift keys are not depressed.
7.	RIGHT SHIFT ON	=	The right shift key is depressed and not yet released.
8.	LEFT SHIFT ON	=	The left shift key is depressed and not yet released.
9.	ALT ON	=	The Alt key (left or right) is depressed and not yet released.
10.	ALT ON	=	The ALT keys are not pressed.

11. SCROLL LOCK ON = The SCROLL LOCK LED is lighted.
(if no such LED, internal status is stored.

12. SCROLL LOCK OFF = The SCROLL LOCK LED is off.
(if no such LED, internal status is stored)

13. NUM LOCK ON = The Num Lock LED is lighted.
Main unit interprets numeric keypad as numbers

14. NUM LOCK OFF = The Num Lock LED is off.
Main unit interprets numeric key pad as cursor.

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
F1	3B	repeatedly 3B	BB
F2	3C	repeatedly 3C	BC
F3	3D	repeatedly 3D	BD
F4	3E	repeatedly 3E	BE
F5	3F	repeatedly 3F	BF
F6	40	repeatedly 40	C0
F7	41	repeatedly 41	C1
F8	42	repeatedly 42	C2
F9	43	repeatedly 43	C3
F10	44	repeatedly 44	C4
F11	57	repeatedly 57	D7
F12	58	repeatedly 58	D8
ESC	01	repeatedly 01	81

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
Caps Lock	3A and toggles Caps Lock	repeatedly 3A and Caps Lock LED unchange	BA and LED Caps Lock unchange
Num Lock	45 and toggles Num Lock	repeatedly 45 and Num Lock LED unchanged	C5 and Num Lock LED unchange
Ctrl (Left)	1D	repeatedly 1D	9D
Ctrl (right)	E0,1D	repeatedly E0,1D	E0,9D
Alt (left)	38	repeatedly 38	B8
Alt (right)	E0,38	repeatedly E0,38	E0,B8

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
* (Numeric KeyPad)	If SHIFT OFF, then send 37 If either Left/right SHIFT ON send 37, If Both SHIFT ON then send no code.	If SHIFT OFF, repeatedly send If either left/right SHIFT ON, repeatedly send 37 If Both SHIFT ON then send no code.	If SHIFT OFF, send B7. If either left/right SHIFT ON, send B7 If Both SHIFT ON then send no code.
/ (Numeric) Key Pad)	If SHIFT OFF, then send E0,35. If Left SHIFT ON then send E0,AA, E0,35. If Right SHIFT ON, then send E0, B6,E0,35. If Both SHIFT ON, then send no code.	If SHIFT OFF, repeatedly send EO,35 If either left/right SHIFT ON, repeatedly send E0,35. If Both SHIFT ON then send no code	If SHIFT OFF, send E0,B5 If Left SHIFT ON, then send E0,B5,E0,2A If Right SHIFT ON, then send E0,B5,E0,36. If Both SHIFT ON, then send no code.

Key description	**Pressed**	**Pressed and hold for certain time (1/2 sec)**	**Released**
Print Screen (sys Req)	If ALT ON, then send 54. If ALT OFF, If SHIFT OFF, send E0,2A, E0,37. If SHIFT ON, send E0,37.	If ALT ON, repeat send 54. If ALT OFF, repeat send E0,37,	If ALT ON, send D4. If ALT OFF, Send E0,B7 E0, AA
Scroll Lock	If Ctrl OFF, then send 46, and toggles SCROLL LOCK LED If Ctrl ON, then send 46, and does not toggle SCROLL LOCK LED.	Repeatedly send 46	Send Co. SCROLL LOCK LED not affected
Pause (Break)	If Ctrl ON, then send E0,46, E0,C6. If Ctrl OFF, then send E1,1D,45, E1,9D,C5.	No further code send.	No Code send

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
→	case (i) NUM LOCK OFF and SHIFT OFF, send E0,4D	case (i) NUM LOCK OFF and SHIFT OFF, repeatedly send E0,4D.	NUM LOCK OFF and SHIFT OFF, send E0,CD.
	case (ii) NUM LOCK OFF, SHIFT ON, If Left SHIFT ON, send E0,AA, E0,4D If Right SHIFT ON, send E0,B6, E0,4D If Both SHIFT ON, send E0,B6 E0,AA,EO 4D.	case (ii) NUM LOCK OFF, SHIFT ON, repeatedly send E0,4D	case (ii) NUM LOCK OFF, SHIFT ON, If Left SHIFT ON, send E0,CD, E0,2A. If Right SHIFT ON, send E0,CD, E0,36. If Both SHIFT ON, send E0,CD, E0,36,E0, 2A.
	case (iii) NUM LOCK ON, SHIFT OFF, send E0,2A, E0,4D	case (iii) NUM LOCK ON, SHIFT OFF, repeatedly send E0,4D.	case (iii) NUM LOCK ON, SHIFT OFF, send E0,CD, E0,AA.
	case (iv) NUM LOCK ON, SHIFT ON, send E0,4D.	case (iv) NUM LOCK ON, SHIFT ON, repeatedly send E0,4D.	case (iv) NUM LOCK ON, SHIFT ON, send E0,CD.

Key description	**Pressed**	**Pressed hold for certain time (1/2 sec)**	**Released**
SHIFT (left)	2A	repeatedly 2A	AA
SHIFT (right)	36	repeatedly 36	B6
Enter (Big)	1C	repeatedly 1C	9C
ENTER (Numeric KeyPad	E0,IC	repeatedly E0,IC	E0,9C
+ (Numeric KeyPad)	4E	repeatedly 4E	CE
-(Numeric KeyPad)	4A	repeatedly 4A	CA

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
Insert	case (i) NUM LOCK OFF and SHIFT OFF, send E0,52.	case (i) NUM LOCK and SHIFT OFF, repeatedly send E0,52.	case (i) NUM LOCK OFF and SHIFT OFF, send E0,D2.
	case (ii) NUM LOCK OFF, SHIFT ON, If Left SHIFT ON, send E0,AA, E0,52 If Right SHIFT ON, send E0,B6, E0,B2. If Both SHIFT ON, SEND E0,B6, E0,AA,E0, 52.	case (ii) NUM LOCK OFF, SHIFT ON, repeatedly send E0,52	case (ii) NUM LOCK OFF, SHIFT ON, If Left SHIFT ON, send E0,D2, E0,2A If Right SHIFT ON, send E0,D2, E0,36. If Both SHIFT ON, send E0,D2, E0,36,E0, 2A.
	case (iii) NUM LOCK ON, SHIFT OFF, send E0,2A, E0,52.	case (iii) NUM LOCK ON, SHIFT OFF, repeatedly send E0,52.	case (iii) NUM LOCK ON, SHIFT OFF, send E0,D2, E0,AA.
	case (iv) NUM LOCK ON, SHIFT ON, send E0,52	case (iv) NUM LOCK ON, SHIFT ON, repeatedly send E0,52.	case (iv) NUM LOCK ON, SHIFT ON, send E0,D2.

Key description	**Pressed**	**Pressed and hold for certain time (1/2 sec)**	**Release**
Delete	case (i) NUM LOCK OFF and SHIFT OFF, send E0,53.	case (i) NUM LOCK OFF adn SHIFT OFF, repeatedly send E0,53.	case (i) NUM LOCK OFF and SHIFT OFF, send E0,D3.
	case (ii) NUM LOCK OFF, SHIFT ON, If Left SHIFT ON, send E0,AA, E0,53. If Right SHIFT ON, send E0,B6, E0,53. If Both SHIFT ON, send E0,B6, E0,AA,E0, 53.	case (ii) NUM LOCK OFF, SHIFT ON, repeatedly send E0,53	case (ii) NUM LOCK OFF, SHIFT ON, If Left SHIFT ON, send E0,D3, E0,2A. If Right SHIFT ON, send E0, D3,E0,36. If Both SHIFT ON, send EO, D3,E0,36, E0,2A.
	case (iii) NUM LOCK ON, SHIFT OFF, send E0,2A, E0,53.	case (iii) NUM LOCK ON, SHIFT OFF repeatedly send E0,53.	case (iii) NUM LOCK ON, SHIFT OFF, send E0,D3, E0,AA.
	case (iv) NUM LOCK ON, SHIFT ON, send E0,53.	case (iv) NUM LOCK ON, SHIFT ON, repeatedly send E0,53.	case (iv) NUM LOCK ON, SHIFT ON, send E0,D3.

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
Home	case (i) NUM LOCK OFF and SHIFT OFF, send E0,47	case (i) NUM LOCK OFF and SHIFT OFF, repeatedly send E0,47.	case (i) NUM LOCK OFF and SHIFT OFF,send E0, C7.
	case (ii) NUM LOCK OFF,SHIFT ON, If Left SHIFT ON, send E0,AA, E0,47 If Right SHIFT ON, send E0,B6, E0,47 If Both SHIFT ON, send E0,B6, E0,AA,E0, A7	case (ii) NUM LOCK OFF, SHIFT ON repeatedly send E0,47	case (ii) NUM LOCK OFF, SHIFT ON, If Left ON, send E0, C7,E0,2A. If Right SHIFT ON, send E0, C7, E0,36. If Both ON, send E0. C7,E0,36. E0,2A.
	case(iii) NUM LOCK ON, SHIFT OFF, send E0,2A,E0, 47.	case(iii) NUM LOCK ON, SHIFT OFF, repeatedly send E0,47.	case (iii) NUM LOCK ON, SHIFT OFF, send E0,C7, E0,AA.
	case (iv) NUM LOCK ON, SHIFT ON, send E0, 47.	case (iv) NUM LOCK ON, SHIFT ON, repeatedly send E0,47.	case (iv) NUM LOCK ON, SHIFT ON, send E0,C7.

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
↓	case (i) NUM LOCK OFF and SHIFT OFF, send E0,50.	case (i) NUM LOCK OFF and SHIFT OFF, repeatedly E0,50.	case (i) NUM LOCK OFF and SHIFT OFF send E0,D0.
	case (ii) NUM LOCK OFF, SHIFT ON, If Left SHIFT ON send E0,AA, E0,50. If Right SHIFT ON send E0,B6, E0,50. IF Both SHIFT ON, send E0,B6, E0,AA,E0,50	case (ii) NUM LOCK OFF SHIFT ON, repeatedly send E0,50	case (ii) NUM LOCK OFF SHIFT ON, If Left SHIFT ON, send E0, D0,E0,2A. If Right SHIFT ON, send E0,D0, E0,36. If Both SHIFT ON, send E0, D0,E0,36, E0,2A.
	case (iii) NUM LOCK ON, SHIFT ON, send E0, 2A,E0, 50.	case (iii) NUM LOCK ON SHIFT OFF, repeatedly send E0.50	case (iii) NUM LOCK ON SHIFT OFF, send E0,D0. E0,AA.
	case (iv) NUM LOCK ON, SHIFT ON,send E0, 50.	case (iv) NUM LOCK ON SHIFT ON, repeatedly send E0,50.	case (iv) NUM LOCK ON, SHIFT ON, send E0,D0.

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
←	case (i) NUM LOCK OFF and SHIFT OFF, send E0,4B.	case (i) NUM LOCK OFF and SHIFT OFF, repeatedly send E0,4B.	case (i) NUM LOCK OFF and SHIFT OFF, send E0,CB.
	case (ii) NUM LOCK OFF,SHIFT ON, If Left SHIFT ON send E0,AA. E0,4B If Right SHIFT ON , send E0,B6, E0,4B If Both SHIFT ON, send E0,B6, E0,AA,E0, 4B.	case (ii) NUM LOCK OFF, SHIFT ON, ON, repeatedly send E0,4B	case (ii) NUM LOCK OFF SHIFT ON, If Left SHIFT ON, send E0,CB. E0,2A. If Right SHIFT ON, send E0,CB, E0,36. If Both SHIFT ON, send E0,CB, E0,36,E0,2A.
	case (iii) NUM LOCK ON, SHIFT OFF,send E0,2A,E0, 4B.	case (iii) NUM LOCK ON SHIFT OFF, repeatedly send E0,4B.	case (iii) NUM LOCK ON SHIFT OFF, send E0,CB. E0,AA.
	case (iv) NUM LOCK ON, SHIFT ON,send E0,4B	case (iv) NUM LOCK ON SHIFT ON, repeatedly send E0,4B.	case (iv) NUM LOCK ON, SHIFT ON, send E0,CB.

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
↑	case (i) NUM LOCK OFF and SHIFT OFF, send E0,48.	case (i) NUM LOCK OFF and SHIFT OFF, repeatedly send E0,48.	case (i) NUM LOCK OFF and SHIFT OFF, send E0,C8.
	case (ii) NUM LOCK OFF,SHIFT ON, If Left SHIFT ON send E0,AA. E0,48 If Right SHIFT ON , send E0,B6, E0,48 If Both SHIFT ON, send E0,B6, E0,AA,E0, 48.	case (ii) NUM LOCK OFF, SHIFT ON, ON, repeatedly send E0,48	case (ii) NUM LOCK OFF SHIFT ON, If Left SHIFT ON, send E0,C8. E0,2A. If Right SHIFT ON, send E0,C8, E0,36. If Both SHIFT ON, send E0,C8, E0,36,E0,2A.
	case (iii) NUM LOCK ON, SHIFT OFF,send E0,2A,E0, 48.	case (iii) NUM LOCK ON SHIFT OFF, repeatedly send E0,48.	case (iii) NUM LOCK ON SHIFT OFF, send E0,C8. E0,AA.
	case (iv) NUM LOCK ON, SHIFT ON,send E0,48	case (iv) NUM LOCK ON SHIFT ON, repeatedly send E0,48.	case (iv) NUM LOCK ON, SHIFT ON, send E0,C8.

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
Page Down	case (i) NUM LOCK OFF and SHIFT OFF, send E0,51.	case (i) NUM LOCK OFF and SHIFT OFF repeatedly send E0,51.	case (i) NUM LOCK and SHIFT OFF, send E0,D1.
	case (ii) NUM LOCK OFF,SHIFT ON, If Left SHIFT ON send E0,AA. E0,51 If Right SHIFT ON , send E0,B6, E0,51 If Both SHIFT ON, send E0,B6, E0,AA,E0, 51.	case (ii) NUM LOCK OFF, SHIFT ON, ON, repeatedly send E0,51	case (ii) NUM LOCK OFF SHIFT ON, If Left SHIFT ON, send E0,D1. E0,2A. If Right SHIFT ON, send E0,D1 E0,36. If Both SHIFT ON, send E0,D1, E0,36,E0,2A.
	case (iii) NUM LOCK ON, SHIFT OFF,send E0,2A,E0, 51.	case (iii) NUM LOCK ON SHIFT OFF, repeatedly send E0,51.	case (iii) NUM LOCK ON SHIFT OFF, send E0,D1. E0,AA.
	case (iv) NUM LOCK ON, SHIFT ON,send E0,51	case (iv) NUM LOCK ON SHIFT ON, repeatedly send E0,51.	case (iv) NUM LOCK ON, SHIFT ON, send E0,D1.

Key description	**Pressed**	**Pressed and hold for certain time (1/2 sec)**	**Released**
Page Up	case (i) NUM LOCK OFF and SHIFT OFF, send E0,49.	case (i) NUM LOCK OFF and SHIFT OFF, repeatedly send E0,49.	case (i) NUM LOCK OFF and SHIFT OFF, send E0,C9.
	case (ii) NUM LOCK OFF,SHIFT ON, If Left SHIFT ON send E0,AA. E0,49 If Right SHIFT ON , send E0,B6, E0,49 If Both SHIFT ON, send E0,B6, E0,AA,E0, 49.	case (ii) NUM LOCK OFF, SHIFT ON, ON, repeatedly send E0,49	case (ii) NUM LOCK OFF SHIFT ON, If Left SHIFT ON, send E0,C9. E0,2A. If Right SHIFT ON, send E0,C9 E0,36. If Both SHIFT ON, send E0,C9, E0,36,E0,2A.
	case (iii) NUM LOCK ON, SHIFT OFF,send E0,2A,E0, 49.	case (iii) NUM LOCK ON SHIFT OFF, repeatedly send E0,49.	case (iii) NUM LOCK ON SHIFT OFF, send E0,C9. E0,AA.
	case (iv) NUM LOCK ON, SHIFT ON,send E0,49	case (iv) NUM LOCK ON SHIFT ON, repeatedly send E0,49.	case (iv) NUM LOCK ON, SHIFT ON, send E0 C9.

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
End	case (i) NUM LOCK OFF and SHIFT OFF, send E0,4F.	case (i) NUM LOCK OFF and SHIFT OFF, repeatedly send E0,4F.	case (i) NUM LOCK OFF and SHIFT OFF, send E0,CF.
	case (ii) NUM LOCK OFF,SHIFT ON, If Left SHIFT ON send E0,AA. E0,4F If Right SHIFT ON , send E0,B6, E0,4F If Both SHIFT ON, send E0,B6, E0,AA,E0, 4F.	case (ii) NUM LOCK OFF, SHIFT ON, ON, repeatedly send E0,4F	case (ii) NUM LOCK OFF SHIFT ON, If Left SHIFT ON, send E0,CF. E0,2A. If Right SHIFT ON, send E0,CF E0,36. If Both SHIFT ON, send E0,CF, E0,36,E0,2A.
	case (iii) NUM LOCK ON, SHIFT OFF,send E0,2A,E0, 4F.	case (iii) NUM LOCK ON SHIFT OFF, repeatedly send E0,4F.	case (iii) NUM LOCK ON SHIFT OFF, send E0,CF. E0,AA.
	case (iv) NUM LOCK ON, SHIFT ON,send E0,4F	case (iv) NUM LOCK ON SHIFT ON, repeatedly send E0,4F.	case (iv) NUM LOCK ON, SHIFT ON, send E0 CF.

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
~ `	29	repeatedly 29	A9
! 1	02	repeatedly	82
@ 2	03	repeatedly	83
# 3	04	repeatedly 04	84
$ 4	05	repeatedly 05	85
% 5	06	repeatedly 06	86
^ 6	07	repeatedly 07	87
& 7	08	repeatedly 08	88
* 8	09	repeatedly 09	89
(9	0A	repeatedly 0A	8A
) 0	0B	repeatedly 0B	8B
_ -	0C	repeatedly 0C	8C
+ =	0D	repeatedly 0D	8D
| \	2B	repeatedly 2B	AB

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
←	OE	repeatedly 0E	8E
Tab ⇤⇥	OF	repeatedly 0F	8F
Q	10	repeatedly 10	90
W	11	repeatedly 11	91
E	12	repeatedly 12	92
R	13	repeatedly 13	93
T	14	repeatedly 14	94
Y	15	repeatedly 15	95
U	16	repeatedly 16	96
I	17	repeatedly 17	97
O	18	repeatedly 18	98
P	19	repeatedly 19	99
{ [	1A	repeatedly 1A	9A

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
}]	1B	repeatedly 1B	9B
A	1E	repeatedly 1E	9E
S	1F	repeatedly 1F	9F
D	20	repeatedly 20	A0
F	21	repeatedly 21	A1
G	22	repeatedly 22	A2
H	23	repeatedly 23	A3
J	24	repeatedly 24	A4
K	25	repeatedly 25	A5
L	26	repeatedly 26	A6
: ;	27	repeatedly 27	A7
“ ‘	28	repeatedly 28	A8

Key description	Pressed	Pressed and hold for certain time (1/2 sec)	Released
Z	2C	repeatedly 2C	AC
X	2D	repeatedly 2D	AD
C	2E	repeatedly 2E	AE
V	2F	repeatedly 2F	AF
B	30	repeatedly 30	B0
N	31	repeatedly 31	B1
M	32	repeatedly 32	B2
 ,	33	repeatedly 33	B3
> .	34	repeatedly 34	B4
? /	35	repeatedly 35	B5
Space Bar	39	repeatedly 39	B9
0 Ins	52	repeatedly 52	D2
. Del	53	repeatedly 53	D3

Key description	**Pressed**	**Pressed and hold for certain time (1/2 sec)**	**Released**
1 End	4F	repeatedly 4F	CF
2 ↓	50	repeatedly 50	D0
3 Pg D	51	repeatedly 51	D1
4 ←	4B	repeatedly 4B	CB
5	4C	repeatedly 4C	CC
6 →	4D	repeatedly 4D	CD
7 Home	47	repeatedly 47	C7
8 ↑	48	repeatedly 48	C8
9 Pg Up	49	repeatedly 49	C9

3.3.3 Keyboard Timing

The typical timing for a single scan code and for a multicode are shown in Fig 3.3 and Fig 3.4 respectively.

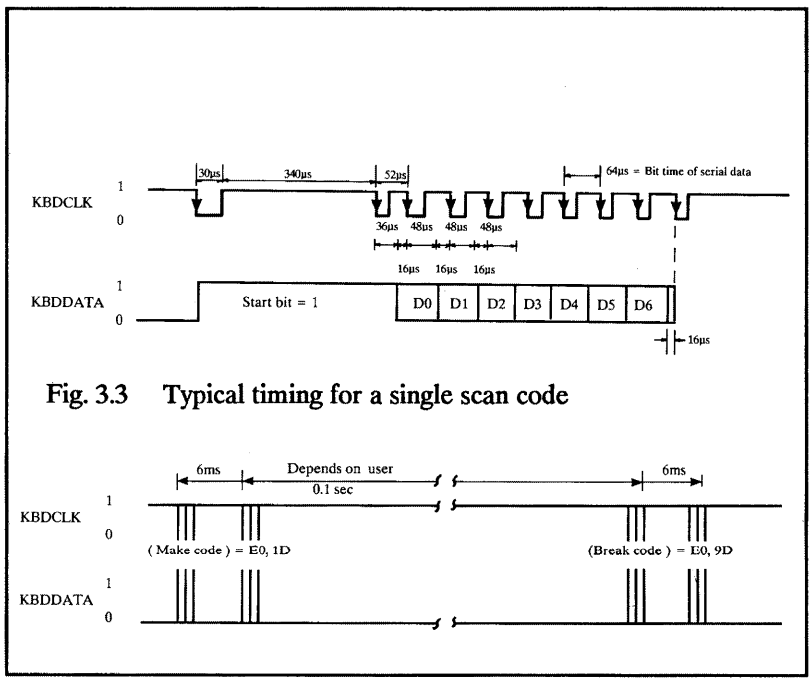
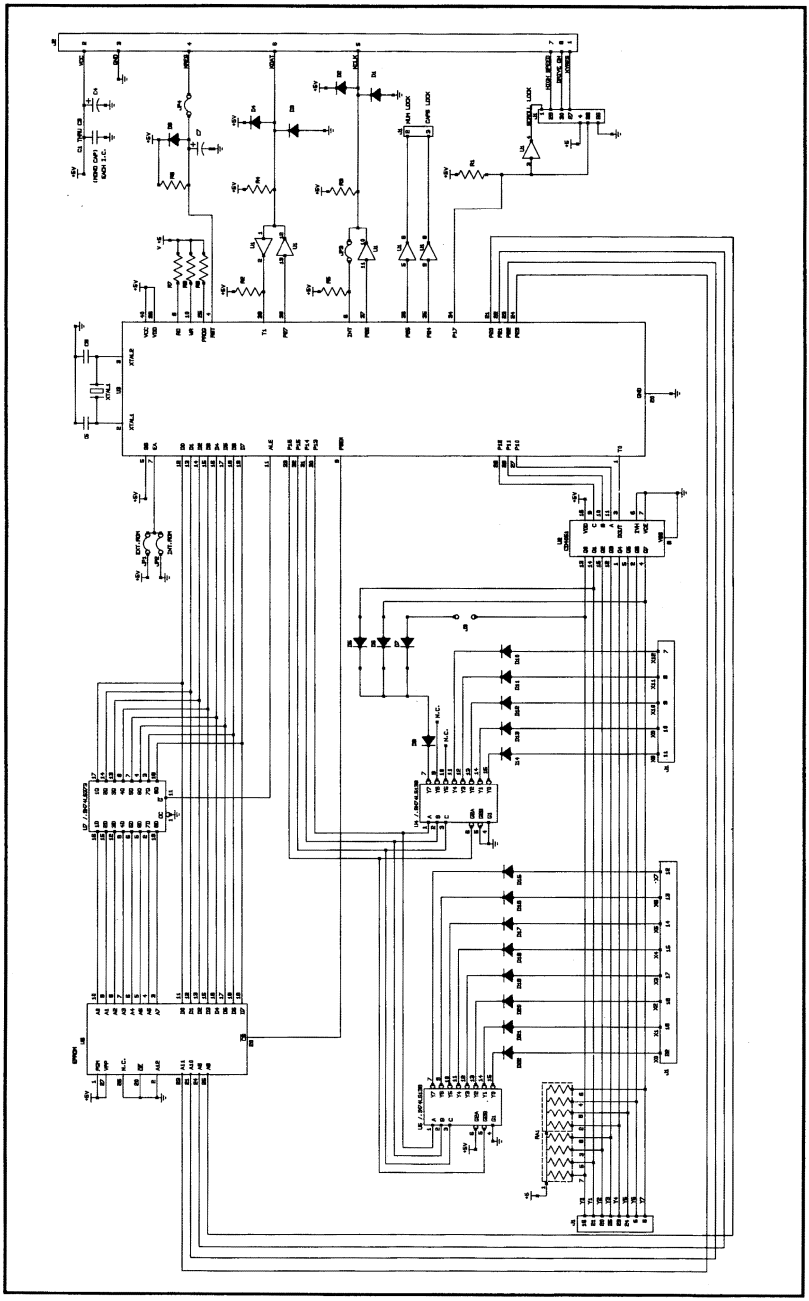


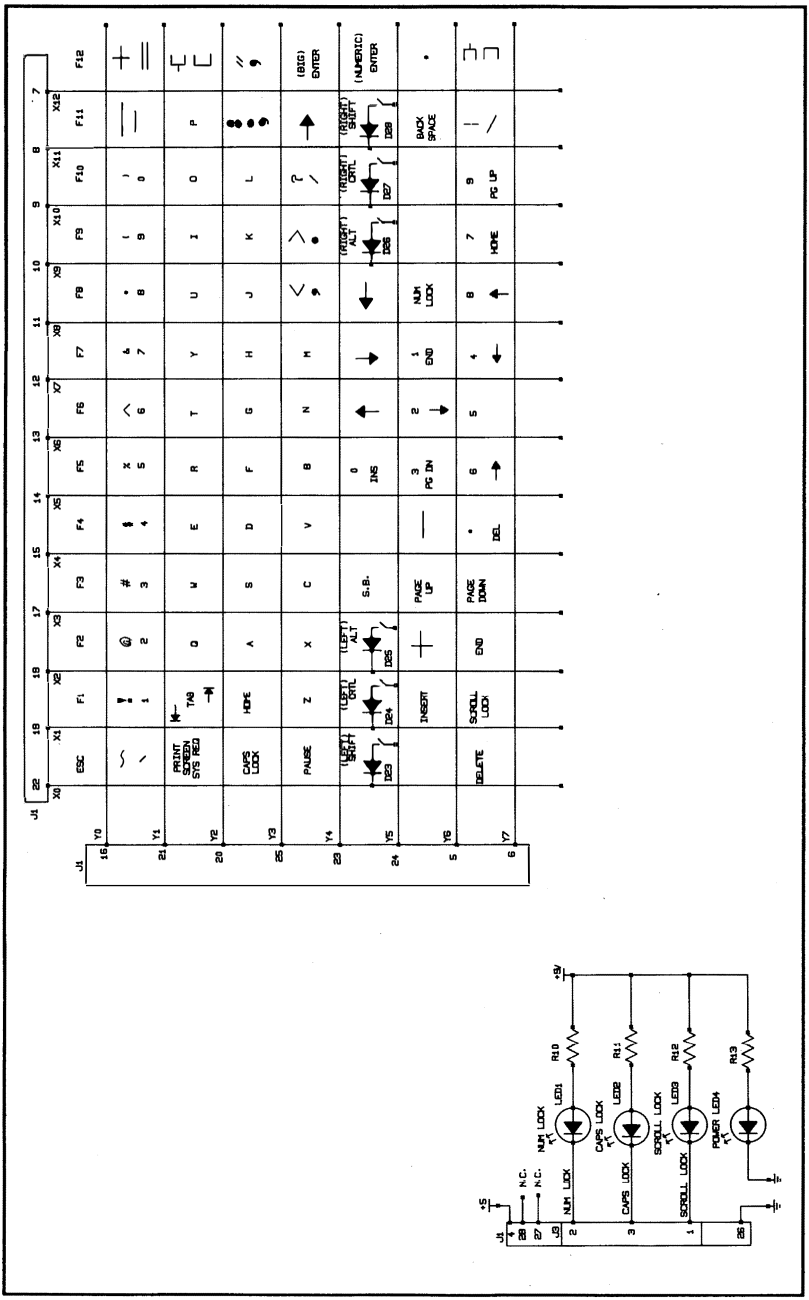
Fig. 3.3 Typical timing for a single scan code

Fig 3.4 Typical timing for multicode generated consecutively.

3.4 Enhanced keyboard interface circuit



3.5 Enhanced keyboard matrix



CHAPTER 4

POWER SUPPLY

4. POWER SUPPLY

4.1 Power supply Specification

Item	Condition*		Min	Type	Max	Unit
Input Voltage	110v Switched		90	110	130	VAC
	220V Switched		180	220	260	VAC
Input Frequency			47		63	Hz
Loading range		5V	3		15	A
		12V	1.5		4.2 *1	A
		-5V	0.0		0.3	A
		-12V	0.0		0.3	A
· Total Regulation	Overall loading and input ranges	5V			+5%	
		12v			+10% 5%	
		-5v			+15%	
		-12V			+15%	
Noise and Ripple		5v			100	MVp-p
		12V			200	MVp-p
		-5V			100	MVp-p
		-12v			200	MVp-p
Efficienty			70%			
Transient A. Overshoot	1K Hz square test wavefrom,, switching from min. to max. other rail kept at max. loading	5V			10%	
		12V			10%	
		-5V			10%	
		-12V			10%	
Transient Response B. Settling Time		5V			10	us
		12V			10	us
		-5V			10	us
		-12V			10	us

Item	Condition*2	Min	Ty0pe	Max	Unit
Overvoltage Protection Threshold	5V			6.5	V
S/C input Power	Any rail shorted to GND			10	W
Inrush current				60	A
Power good Signal	VOH	3.0			V
	VOL			0.4	V
	IOL			4	MA
	IOH			-1.0	MA
	t1	100		500	MScc
	t2			5	uscc
Hi-Pot Potential	Between Pri-Scc For 1 min. Pri-E	2500 2500			VDC VDC
EM1	Meets FCC class B				
Safety	UL File E104979 CSA File LR67961				
Mechanical Dimension	Compatible with standard PC XT Switching power Supply				

*1 This rating is for Turbo XT and Turbo XT/2 UL version. For Turbo XT and Turbo XT/2 CSA version, it should be 5.6A. For Turbo XT/3 both UL and CSA version, it should be 5.2A

*2 Condition: Normal line
max, load
unless otherwise specified

4.2 Output Connector Pin Out

The power supply connectors and pin assignments is shown in Fig 4.1

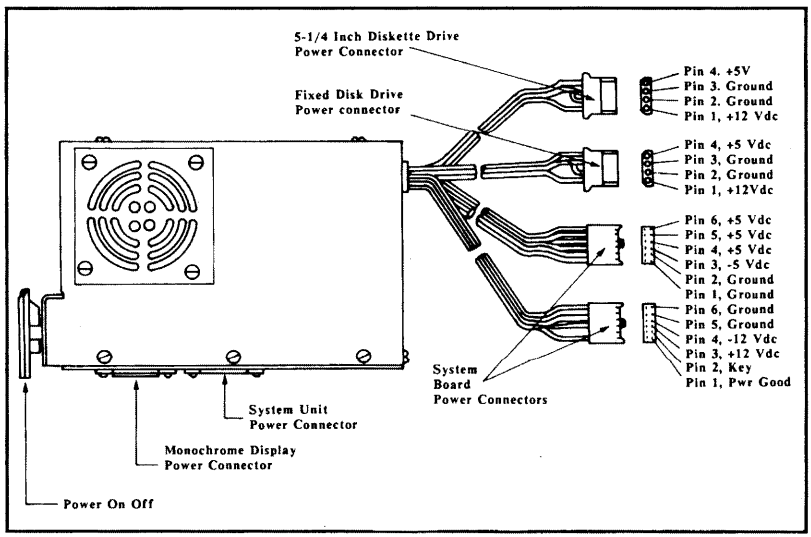


Fig 4.1 Power Supply and connectors

Note: *Power supply of Turbo XT/3 provides five power connectors. However, power supply of Turbo XT and Turbo XT/2 may have four power connectors only.*

The color of the wire of different pin out is as follow:

Pin Out	Color
+5V	red
+12V	yellow
-5V	white
-12V	blue
GND	black
Power good	orange

4.3 Power Consumption

The Power consumption estimation of the LASER Turbo XT or Turbo XT/2 is summarized in the following table.

Supply voltage (V)	5	12
Supply current (A)	15	4.2
Current taken by (A) System board	2	-
Current taken by 1st (A) 5" 1/4. drive	0.24	0.37
Current taken by 2st (A) 5" 1/4. drive	0.24	0.37
Current taken by one (A) 20 MB Hard Disk	0.8	0.9
Current available for slots (8slots) (A)	11.72	2.56
Average current available for each slot (A)	1.46	0.32

The power consumption estimation of LASER Turbo XT/3 is shown below:-

Supply voltage (V)	**5**	**12**
Supply current (A)	15	5.2
Current taken by (A) system board	2	-
Current taken by (A) 5 1/4" Drive	0.24	0.37
Current taken by (A) 3 1/2" Drive	0.12	0.3
Current taken by one (A) 20MB Hard Disk	0.8	0.9
Current available for slots (8 slots) (A)	11.84	3.63
Average current available for each slot (A)	1.48	0.45

CHAPTER 5

SYSTEM BIOS

5. SYSTEM BIOS

5.1 Interrupt Calls Overview

The BIOS routines are called through the CPU software interrupt. The parameters are passed using the CPU registers. The following section provides an overview on the various routines.

1. Interrupt Hex 0 - Divide by Zero

2. Interrupt Hex 1 - Single Step

3. Interrupt Hex 2 - Nonmaskable

   When this interrupt is called, the interrupt handler will print a parity error message. The segment addresses will be also be printed.

4. Interrupt Hex 3 - Breakpoint

5. Interrupt Hex 4 - Overflow

6. Interrupt Hex 5 - Print Screen

   This interrupt is used to copy the content of the screen to the printer. The current cursor position will be saved and restored when printing is completed.

7. Interrupt Hex 6 - Reserved

8. Interrupt Hex 7 - Reserved

9. Interrupt Hex 8 - Time of Day

   The interrupt handler handles the timer interrupt from channel 0 of the timer. There are 18.2 interrupts per second. The interrupt handler keeps a count of interrupts since power on time. This can be used as the time of day. The interrupt handler also decrements the motor control count of the diskette, and turn off the diskette motor, and reset the motor running flags when the count reach zero.

10. Interrupt Hex 9 - Keyboard

    This interrupt handles keyboard interrupt.

11. Interrupt Hex A - Reserved

12. Interrupt Hex B - Communications

13. Interrupt Hex C - Communications

14. Interrupt Hex D - Disk

15. Interrupt Hex E - Diskette

    This interrupt handle the diskette interrupt.

16. Interrupt Hex F - Printer

17. Interrupt Hex 10 - Video
    This interrupt provides the CRT interface

18. Interrupt Hex 11 - Equipment check
    This interrupt handler reports the configuration of the system.

19. Interrupt Hex 12 - Memory
    This interrupt handler determines the amount of memory in the system.

20. Interrupt Hex 13 - Diskette Disk
    This interrupt provides access to 5 1/4" diskette drive.

21. Interrupt Hex 14 - Communications
    This interrupt handler provides byte stream I/O to the communication ports.

22. Interrupt Hex 15 - Cassette
    Dummy cassette I/O routine. Always return the error code "invalid command".

23. Interrupt Hex 16 - Keyboard
    This interrupt provides Keyboard support.

24. Interrupt Hex 17 - Printer
This interrupt provides communication with the printer.

25. Interrupt Hex 18 - Resident BASIC

26. Interrupt Hex 19 - Bootstrap

This interrupt handler is the boot strap loader which perform the following procedures.

- The fixed disk BIOS substitutes the interrupt 19 Boot strap vector by a pointer to the boot routine.

- The default disk and diskette parameter vectors is reset.

- The boot block from cylinder 0 sector 1 of the device will be read in.

- The Bootstrap sequence is:
> Try to load from the diskette into the boot location (0000:7C00) and transfer control there
> If the diskette fails, the fixed disk is tried for a valid bootstrap block. A valid boot block on the fixed disk consists of the bytes 055H OAAH as the last two bytes of the block.

27. Interrupt Hex 1A - Time of Day

This interrupt handler set and read the clock.

28. Interrupt Hex 1B - Keyboard Break

This interrupt handler will be called when the Ctrl and Break keys on the keyboard are pressed.

29. Interrupt Hex IC - Timer Tick

This interrupt handler will be called from the timer interrupt service routine.

30. Interrupt Hex 1D - Video Parameters

This interrupt vector points to a table containing the parameters for initialing the 6845 on the display adapter.

31. Interrupt Hex IE - Diskette parameter

    This interrupt vector points to a table containing the parameters used by the diskette drive.

32. Interrupt Hex 1F - Graphics Character Extensions.

33. Interrupt Hex 40 - Reserved

    When an Fixed Disk Drive Adapter is installed, this interrupt is used to revector the diskette pointer.

34. Interrupt Hex 41 - Fixed Disk Parameters

    This interrupt vector points to a table containing the parameters used by the fixed disk drive.

5.2 Interrupt Call Summary

Service	Interrupt (Hex)	Register Input	Output	Description
Print screen	05	AH=05	n/a	Send screen contents to printer. Status and result byte at low-memory address hex 500 (0050:0000)
Video Services				
Set video mode	10	AH=OO AL=Video mode	none	Video modes in AL: 00:40 X 25 text, 16 B/W 01:04 X 25 text, 16/8 color 02:80 X 25 text, 16 B/W 03:80 x25 text, 16/8 color 04:320 X 200 graphics, 4 color 05:320 X 200 graphics, 4 B/W 06:640 X 200 graphics, B/W 07:80 X 25 text, B/W
set cursor size	10	AH=01 CH=starting scan line CL=ending scan line	none	Color/graphics Adapter uses lines 0-7 Monochrome Adapter uses lines 0-13

Set cursor position	10	AH = 02 BH = display page number DH = row DL = column	none
Read cursor position	10	AH = 03 BH = display Page number	CH = starting scan line CI = ending scan line DH = row DL = column
Read light-pen position	10	AH = 04	AH = pen trigger signal BX = pixel column CH = pixel row DH = character row DL = character column
Set active display page	10	AH = 05 AL = page number	
Scroll window up	10	AH = 06 AL = lines to scroll up BH = filer attribute CH = upper row CL = left column DH = lower row DL = right column	none
Scroll window down	10	AH = 07 AL = lines to scroll down BH = filler attribute CH = upper row CL = left column DH = lower row DL = right column	none
Read character and attribute	10	AH = 08 BH = display page number	AH = character AL = attribute
Write character and *attrubute	10	AH = 09 AL = character BH = page number BL = attribute CX = number of characters to repeat	none
Write character	10	AH = 0A AL = character BH = page number BL = color in graphics mode CX = count of characters	none
Set color palette	10	AH = 0B BH = palette color ID BL = color to be used with palette ID	none
Write pixel dot	10	AH = OC AL = color CX = pixel column DL = pixel row	none

Read pixel dot	10	AH=0D CX=pixel column DL=pixel row	AL=color read	
Write character	10	AH=0E AL=character BL=color for TTY graphics mode	none	
Get current video mode	10	AH=OF	AH=width in characters AL=video mode BH=page number	
Equipment-List Service				
Get list of peripheral attached equipment	11	none	AX=equipment list, bit-coded	Bit settings in AX: 00=disk drive 01=math coprocessor 02, 03=system board 04, 05=initial video mode 00=unused; 01=40 X 25 color; 10=80 X25 color: 11=80 X 25 B/W 06, 07=number of disk drives 08=DMA present? 00=yes; 01=no 09, 10, 11=number of RS-232 cards in system 12=game I/O attached 13=serial printer attached 14, 15=number of printers attached
Memory Service				
Get usable memory size (in K-bytes)	12	none	AX=memory size	
Diskette Service				
Reset diskette system	13	AH=00	none	
Get diskette status	12	AH=01	AL=Status code	Status values: AL=1:bad command AL=2:address mark not found AL=3: write *atempted on write-protected disk AL=4: sector not found AL=6: diskette removed AL=8: DMA overrun AL=9: DMA across 64K boundary AL=10: bad CRC AL=20: NEC controller failed AL=40: seek failure AL=80: time out

Read diskette sectors	13	AH=02 AL=number of sectors CH=track CL=sector number DH=head number DL=drive number ES:BX=pointer to buffer	CF=success/ failure signal AH=status code AL=number of number sectors read	Status codes in AH: see diskette service 01
Write diskette sectors	13	AH=03 AL=number of sectors CH=track CL=sector number DH=head number DL=drive number ES:BX=pointer to buffer	CF=success/ failure flag AH=status code AL=number of sectors written	Status codes in AH: see diskette service 01
Verify diskette sectors	13	AH=04 AL=number of sectors CH=track number verified CL=sector number DH=head number DL=drive number	CF=success/ failure (signal) AH=status code AL=number of sectors	Status codes in AH: see diskette service 01
Format diskette track	13	AH=05 AL=number of sectors AH=status code CH=track number DH=head number DL=drive number ES: BX=pointer to list of 4-byte address fields: Byte 1=track Byte 2=head Byte 3=sector Byte 4=bytes/sector	CF=success/ failure signal	Status codes in AH: see diskette service 01

Serial Port Services

Initial-ize serial port parameters	14	AH=00 DX=serialstatus PORT number	AX=serial port 00,01=word length	Status bit settings: 10=7 BITS; 11-8 BITS 02=stop bits: 0=1; 1=2 03,04=parity: 00, 01=none; 01=odd; 11=even 05, 06, 07= band rate; 000=110; 001=150; 010=360; 011=600; 100=1,200; 101=2,400; 110=4,800; 111=9,600

Send out one character	14	AH=01 AL=character code DX=serial port number	AH=success/ failure status AL=modem status	AH bit settings: 00=data ready; 01=overrun error; 02=parity error; 03=framing error; 04=break detected; 05=transmission buffer register empty; 06=transmission shift register empty; 07=time out AL bit settings: 00=delta clear-to-send; 01=delta data-set-ready; 02=trailing edge ring detected; 03=change, receive line signal detected 04=clear-to-send; 05=data-set-ready; 06=ring detected; 07=receive line signal detected
Receive one character	14	AH=02 DX=serialfailure status port number	AH=success/ see serial port code AL=character	Status bit settings: service 01
Get serial port status		14 AH=03 AX=status code		Status code bit settings: see serial port service 00
Cassette Tape services		Dummy service, *alway returns error code of invalid command.		

Keyboard Services

Read next keyboard character	16	AH=00		AH=scan code (auxiliary byte) AL=character code (main byte)
Report whether character ready	16	AH=01		ZF=ready or not signal AH=scan code (auxiliary byte) AL=character code (main byte)
Get shift status	16	AH=02	AL=shift status bits	Shift status bits: Bit 0=1: right Shift Bit 1=1: left Shift depressed Bit 2=1: Ctrl depressed Bit 3=1: Alt depressed Bit 4=1: Scroll Lock active Bit 5=1: Num Lock active Bit 6=1: Caps Lock active Bit 7=1: Insert state active

Printer Services				
Send one byte to printer	17	AH=00 AL=character	AH=success/ failure	Status not settings: 0=time out Status code 1=unused 2=unused 3=1: I/O error 4=1: selected 5=1: out of paper 6=1: acknowledge 7=1: not busy
Initial-ize printer	17	AH=01	AH=status code	Status code bit settings: see printer service 00
Get printer status	17	AH=02	AH=status code	Status code bit settings: see printer service 00
Miscellaneous Services				
Switch control to BASIC	18	none	n/a	No return, so no possible output
Reboot computer	19	none	n/a	No return, so no possible output
Time-of-Day Services				
Read the current clock count	1A	AH-00	AL=midnight signal CX=tick count, high portion DX=tick count, low portion	
Set current clock count	1A	AH=01 CX=tick count, high portion DX=tick count, low portion	none	

5.3 Laser Turbo XT,TURBO XT/2, AND TURBO XT/3 BIOS Error Message

BEEPS	DESCRIPTION
1 long + 1 short	Base 64K RAM (00000H-0FFFFH) isn't usable. SOLUTION - Check RAM chips
1 long + 2 short	Video switches wrong for the installed adapter. SOLUTION - Check DIP switches and video selection.

1 long + 5 short	BIOS ROM check sum is incorrect. (Bad EPROM) SOLUTION - Replace BIOS chip.

Display Messages

VIDEO ERROR

BIOS couldn't find the display adapter requested by the DIP switches. BIOS is instead using the adapter it did find. SOLUTION - Check DIP switches and video card.

KEYBOARD ERROR 0100

Keyboard did not respond.
(No interrupt) SOLUTION - Check internal connector on the keyboard.

KEYBOARD ERROR 02XX

Keyboard returned wrong test code xx.
SOLUTION - Replace keyboard.

KEYBOARD ERROR 04XX

Keyboard interrupt would not clear.
SOLUTION - Check Gate Array on Motherboard or replace the keyboard.

MEMORY ADDR ERROR SBBBB, DD

Problem with memory addressing. Possibly unconnected RAM legs or shorted address lines.
SOLUTION - Check the RAM chips (replace one at a time). If BBBB=0000 then the problem was detected on address bits A16-A 19; "S" value (0-9) indicates the lowest segment which failed. If BBBB is non-zero, then the problem was found on address lines A0-A15 of the segment "S". The "DD" tells which data bits were wrong.

MEMORY ERROR SBBBB,DD

Other memory problem. The "S" is the 64K segment (0-9). "BBBB" = the offset where the error was found. "DD" = data error bits.

NOTE: The BIOS will not test memory beyond an error and will reduce memory size to exclude the faulty memory.

If memory size is displayed with a decimal point like this:

SYSTEM MEMORY SIZE = 256K

Means that DIP switch #1 is on, and memory beyond 256K will always be ignored. SOLUTION - Check DIP switches.

DRIVE A ERROR XX

"XX" is the INT 13 error code. If "XX" = 80 Time out (no interrupt, missing, or bad adapter) "XX"=40 Seek error (track 0 not found, missing drive) "XX"=20 Bad NEC controller chip.
SOLUTION - Check all plugs and cables on drive. Check DIP switches on motherboard. Make sure drive select switch is correct. Replace controller card. Replace disk drive.

CHAPTER 6

EMS DRIVER

6. EMS DRIVER

6.1 PROGRAMS INSIDE THE EMS DRIVER PROGRAM DISKETTE

EMM.SYS - The expanded memory manager driver program
This is the driver program for using the expanded memory. It must be installed before the expanded memory can be used.

ERAMDISK.SYS - the RAM disk driver program for the expanded memory.
This is the driver program for implementing a RAM disk in the expanded memory. The RAM disk has a drive ID which is the first unused drive ID in your computer system. For example, if your system has two floppy disk drives, the drive ID of the RAM disk will be C:. If your system has two floppy disk drives and one hard disk, the drive ID of the RAM disk will be D:. You need not change the setting of the DIP switch in your computer mainboard as you implement a RAM disk.

CRAMDISK.SYS - The RAM disk driver program for the conventional memory.

This RAM disk driver program is similar to ERAMDISK.SYS except that the RAM disk occupies conventional memory. The naming of the RAM disk drive ID is the same as that in ERAMDISK. SYS. If both ERAMDISK.SYS and CRAMDISK.SYS are implemented, they will have separate drive IDs. If the CRAMDISK. SYS is implemented, some application programs (e.g. SYMPHONY) which requires large conventional memory size cannot be run.

6.2 PREPARING A EMS SYSTEM DISKETTE

To prepare a system diskette with the EMS driver programs, copy the three driver programs to a boottable system diskette. To copy the driver programs to your system diskette, put your system diskette in drive A: and the EMS driver program diskette in drive B:. Enter the following command.

COPY B: *.SYS A: <CR>

Before you can use the driver programs, you have to create a CONFIG.SYS file in your system diskette. The function of the CONFIG.SYS file is to load the device driver programs at boot time. You can enter the following commands to create a CONFIG.SYS file.

```
COPY CON: A: CONFIG.SYS <CR>
DEVICE = EMM.SYS M3 IO <CR>
DEVICE = ERAMDISK.SYS 512 <CR>
DEVICE = CRAMDISK.SYS 128 <CR>
<F6> <CR>
```

Remark:
<CR> is the ENTER key and <F6> is the F6 function key. The above CONFIG.SYS file is only an example. The entries M3, IO, 512, 128 are parameters for the device drivers. They may be varied for different system configurations or applications. If a RAM disk for conventional memory is not required, the command line DEVICE=CRAMDISK.SYS can be omitted. The command line DEVICE = EMM.SYS must be entered before DEVICE = ERAMDISK.SYS.

Parameters in the device drivers:

EMM.SYS
Format: DEVICE=EMM.SYS Ma Ib [Ib...]

M is the parameter heading defining the starting frame address of the memory in the EMS card. The 'a' after M represents a number which can be 0 to 7.

M parameter	Starting frame address (in Hex)
M0	C4000
M1	C8000
M2	CC000
M3	D0000
M4	D4000
M5	D8000
M6	DC000
M7	E0000

The M parameter can be defined in any of the above values but you must make sure the address space of the EMS memory does not conflict with the interface card with Read Only Memory (ROM). The EMS card occupies 64K address space starting from the frame address (i.e. if M0 is defined, EMS card occupies address C4000-D3FFF). If your system contains a hard disk controller card which has a interface ROM with address C8000-CFFFF, parameter M0 and M1 should not be used. It is recommended to use parameter M3, since the address space does not have conflict with most common interface card.

I is the parameter heading defining the I/O port address of the EMS card installed. The 'b' after I represents a number which can be 0 to 6.

I parameter	I/O port EMS board (in Hex)	EMS 1	DIP 2	Switch 3
I0	208	OFF	ON	ON
I1	218	ON	OFF	ON
I2	258	OFF	OFF	ON
I3	268	ON	ON	OFF
I4	2A8	OFF	ON	OFF
I5	2B8	ON	OFF	OFF
I6	2E8	OFF	OFF	OFF

You should define the I parameter according to the DIP switch setting. If your computer system has installed more than one EMS cards (when you fill up more than 2 banks of RAM, you should configure the expanded memory as two cards), the DIP switch setting on each EMS card must be different. You should define one I parameter for one EMS card, two I parameters for two EMS cards installed and so forth. For example, if you have four EMS cards installed, you can define the parameters as follows.

DEVICE=EMM.SYS M3 I0 I1 I2 I3

ERAMDISK.SYS
Format: DEVICE=ERAMDISK.SYS nnnn

nnnn represents a number which defines the RAM disk size in Kbyte of memory. The minimum number is 16 and the maximum number depends on the expanded memory size in your system. If four banks are fully filled with RAM, there are a total of 1024 Kbyte of expanded memory. If these are still not enough for your uses, you can purchase our Expanded Memory card which allows expansion to a maximum of 2 Mbyte per card. (Note: If your system diskette is MSDOS version 2.0 or 2.1 the RAM disk size cannot be defined more than 2048. If your system diskette is MSDOS version 3.0, 3.1, 3.2 or later version, the RAM disk size can be defined up to 8192.

CRAMDISK.SYS
Format: DEVICE=CRAMDISK.SYSnnn

nnn represent a number which defines the RAM disk size in Kbyte of memory. The minimum number is 16 and the maximum number depends on the available conventional memory size. If your application program requires large memory size, it is not recommended to implement this RAM disk.

6.3 PROGRAMMING THE EXPANDED MEMORY

6.3.1 PROGRAMMING GUIDELINE

When using the expanded memory, the programmer should assumes the following:

- There will be more than one expanded memory board.
- Other resident programs may also use expanded memory.
- Program cannot rely on the value of certain register after a function call.
- The size of each page is 16K bytes.
- Four 16K-byte pages can be mapped into a 64K byte region. The starting address of this 64K region is returned by EMM function 2. The 64K bytes region is called page frame.
- The stack should not be located in the expanded memory.
- Since the EMM uses INT 67H, other programs should not use this interrupt vector.
- After testing the presence of the EMM, the page frame base address should be requested.
- The number of free 16K-byte page should be requested so that the maximum number of pages the program can allocated can be determined.
- The EMM functions provide a set of standard expanded memory functions. Programs that deal directly with the hardware or that don't adhere to the specification will have compatibility problem.

6.3.2 Checking the Presence of EMM

There are two methods to check the presence of EMM.

- Issue an open request (MS-DOS function 3DH) using the name of the EMM driver "EMMXXXX0". If the request is successful, issue an 'I/O control for device' command (MS-DOS function 44H) with a 'get device information' command. If the status returned in register AL is 0FFH, then the driver is present. After that, a 'close file handle' command (MS-DOS function 3EH) should be issued to close the EMM device driver.

- Use the INT67H vector to check the device header. If the EMM is present, at offset 0AH of the header will have the string EMMXXXX0. This method must be use if the called program is a device driver or it interrupt DOS during file system operation.

6.3.3 EMM Functions

After ensuring that the Expanded Memory Manager (EMM) is present, an application program communicates with the EMM directly via a software interrupt. The calling sequence for the EMM is:

```
mov     ah, function        ;  AH contains the function number
                            ;  other registers are loaded with
                            ;  function-specific arguments.

int     67h                 ;  transfer to Expanded Memory
                               Manager.
```

If an EMM call is successful, the value zero is returned in register AH; otherwise, AH will contain an error code.

Int 67H
EMS Function 01H(1)
Get status

Tests whether the EMM and expanded memory hardware is working properly.

INPUT	AH	=	40H	
OUTPUT	AH	=	status	
			00H	function successful
			80H	internal error in EMM software
			81H	malfunction in expanded memory hardware
			84H	function requested by application not defined

Int 67H (103)
EMS Function 02H (2)
Get page frame segment

Get the segment address of the page frame used by the EMM

INPUT	AH	=	41H	
OUTPUT	if OK			
	AH	=	00H	
	BX	=	segment of the page frame	
	If failed:			
	AH	=	error code	
			80H	internal error in EMM software
			81H	malfunction in expanded memory hardware
			84H	function requested by application not defined

Int 67H (103)
EMS Function 03H (3)
Get unllocated page count

Get the total number of pages present in the system, and the number of those pages that are free.

Input	AH	=	42H
OUTPUT	If ok		
	AH	=	00H
	BX	=	unllocated pages
	DX	=	total number of pages in the system
	If failed:		
	AH	=	ERROR CODE
			80H internal error in EMM software
			81H malfunction in expanded memory hardware
			84H function requested by application not defined

Int 67H (103)
EMS Function 04H (4)
Allocate Pages

Request the EMM for using the expanded memory, obtains a handle and has a certain number of logical pages allocated under the control of this handle.

INPUT	AH	=	43H
	BX	=	number of logical pages to allocate
OUTPUT	If OK		
	AH	=	00H
	DX	=	handle

If failed:

AH	=	error code	
		80H	internal error in EMM software
		81H	malfunction in expanded memory hardware
		84H	function requested by application not defined
		85H	no more handles available
		87H	allocation request specified more logical pages than are physically available in system; no pages allocated
		88H	allocation request specified more logical pages than are currently available in system (request does not exceed physical pages that exist, but some are already allocated to other handles); no pages allocated
		89H	Zero pages requested

Int 67H (103)
EMS Function 05H (5)
Map Handle page

Maps logical pages of expanded memory assigned to a handle onto one of the four physical pages.

INPUT	AH	=	44H
	AL	=	physical-page number (0-3)
	BX	=	logical-page number
	DX	=	handle

OUTPUT	AH	=	status	
			00H	function successful
			80H	internal error in EMM software
			81H	malfunction in expanded memory hardware
			83H	invalid handle
			84H	function requested by application not defined
			8AH	logical page requested to be mapped is outside range of logical pages assigned to handle
			8BH	illegal physical-page number in mapping request (not in range 0-3)

Int 67H (103)
EMS Function 06H (6)
Deallocate Pages

Deallocates the logical pages of expanded memory currently allocated to a handle,

INPUT	AH	=	45H	
	DX	=	EMM handle	
OUTPUT	AH	=	status	
			00H	function successful
			80H	internal error in EMM software
			81H	malfunction in expanded memory hardware
			83H	invalid handle
			84H	function requested by application not defined
			86H	error in save or restore of mapping context

Int 67H (103)
EMS Function 07H (7)
Get EMM version

Returns the version number of the EMM software.

INPUT AH = 46H

OUTPUT If OK

AH = 00H
AL = EMM version number in BCD format. The upper four bits contain the integer digit. The lower four bits contain the fractional digit.

If failed:
AH = error code

80H	internal error in EMM software
81H	malfunction in expanded memory hardware
84H	function requested by application not defined

Int 67H (103)
EMS Function 08H (8)
Save Map

Save the contents of the expanded memory page-mapping registers on the expanded memory boards, which belong to a EMM handle.

INPUT AH = 47H
DX = handle

OUTPUT	AH	=	status	
			00H	function successful
			80H	internal error in EMM software
			81H	malfunction in expanded memory hardware
			83H	invalid handle
			84H	function requested by application not defined
			8CH	page-mapping hardware state save area is full
			8DH	save of mapping context failed, save area already contains context associated with requested handle

Int 67H (103)
EMS Function 09H (9)
Restore page map

Restores the contents of all expanded memory hardware page-mapping registers to the values for particular handle.

INPUT	AH	=	48H
	DX	=	EMM handle

OUTPUT	AH	=	status	
			00H	function successful
			80H	internal error in EMM software
			81H	malfunction in expanded memory hardware
			83H	invalid handle 84H function requested by application not defined
			8EH	restore of mapping context failed; save area does not contain context for requested handle.

Example: Restore the EMS mapping state for the currently executing program.

```
                mov     ah,48h          ;48H = EMM Function 9
                mov     dx,handle       ;DX = handle from Function 4
                int     67h             ;transfer to Manager.
                or      ah,ah           ;test status.
                jnz     emm-error       ;AH < > 0 if error
                .
emm-error:      .
                .
handle          dw      0
```

Int 67H (103)
EMS Function 0AH (10)
Reserved

Int 67H (103)
EMS Function 0BH (11)
Reserved

Int 67H (103)
EMS Function 0CH (12)
Get Handle count

Gets the number of active EMM handles.

INPUT AH = 4bh

OUTPUT If OK
AH = 00h
BX = number of EMM handles

If failed:
AH = error code

80H	internal error in EMM software
81H	malfunction in expanded memory hardware
83H	invalid handle
84H	function requested by application not defined

Int 67H (103)
EMS Function 0DH (13)
Get EMM Handle Pages

Returns the number of logical expanded memory pages allocated to a specific EMM handle.

INPUT AH = 4CH
DX = EMM handle

OUTPUT If OK
AH = 00H
BX = number of logical pages

If failed:
AH = error code

80H	internal error in EMM software
81H	malfunction in expanded memory hardware
83H	invalid handle
84H	function requested by application not defined.

Int 67H (103)
EMS Function 0EH (14)
Get All EMM Handle Pages

Returns an array of all the active handles and the number of logical expanded memory pages allocated to each handle.

INPUT
AH = 4DH
ES:DI = segment:offset of array to receive information

OUTPUT
If OK
AH = 00h
BX = number of active EMM handles. Each entry in the array is composed of two words, the first contains the EMM handle while the second contains the number of pages allocated to that handle.

If failed:
AH = error code

80H	internal error in EMM software
81H	malfunction in expanded memory hardware
84H	function requested by application not defined

Int 67H (103)
EMS Function 0FH (15)
Get / Set Page Map

Save or sets the contents of the EMS page-mapping registers on the expanded memory boards.

INPUT AH = 4EH
AL = 00H if getting mapping registers into array
01H if setting mapping registers from array
02H if getting and setting mapping registers in one operation
03H if returning size of page-mapping array
DS:SI = segment:offset of array holding information subfunction 01H, 02H)
ES:DI = segment:offset of array to receive information (subfunction 00H, 02H)

OUTPUT If OK

AH = 00H
AL = bytes in page-mapping array (subfunction 03H only)

Array pointed to by ES:DI receives mapping information (subfunctions 00H and 02H)

If failed:
AH = error code
80H internal error in EMM software
81H malfunction in expanded memory hardware
84H function requested by application not defined
8FH subfunction parameter not defined

CHAPTER 7

SERVICING

7. SERVICING

7.1 Circuit Description

7.1.1 Oscillator Circuit

Various system timing signals are generated by two crystal oscillators. The circuit of the oscillators are shown in Fig 7.1

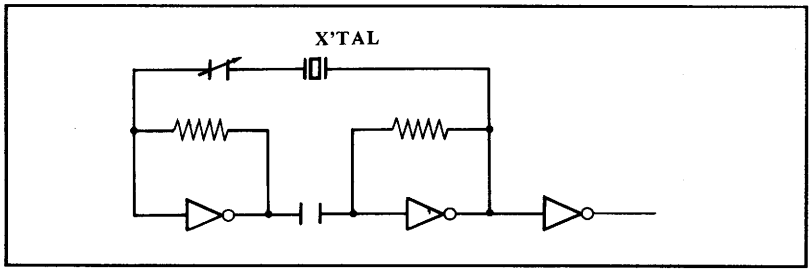
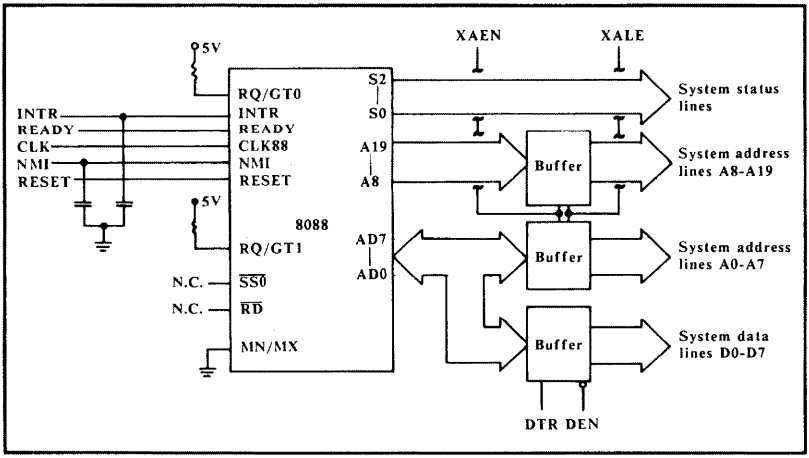


Fig 7.1 Schematic diagram of the crystal oscillator

7.1.2 CPU & Buffers

The CPU is a 8-bit data bus (for 8088-1) or 16-bit data bus (for 8086-1) and 16-bit internal architecture microprocessor builds on HMOS technology. The CPU can be run at a clock frequency of 10MHz with 33% duty cycle, this signal is obtained from Gate Array A1. Fig 7.2 shows the interface to the 8088-1 CPU. Fig 7.3 shows the interface to 8086-1 CPU.

Fig 7.2 Interface to 8088-1 CPU



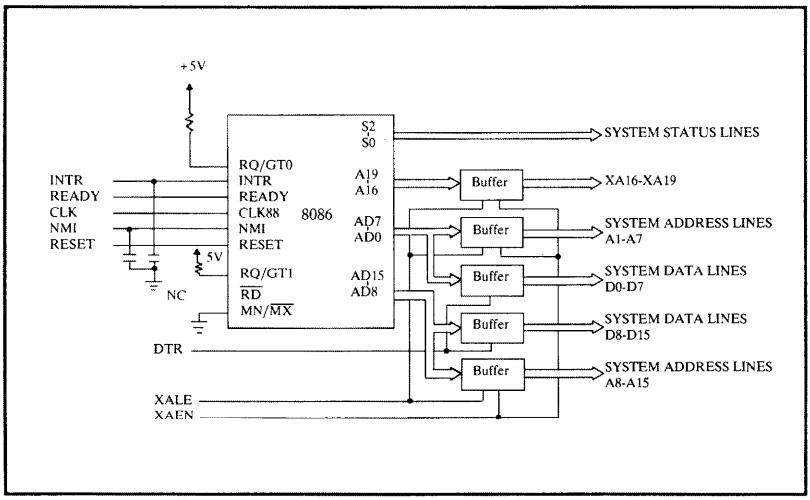


Fig 7.3 Interface to 8086-1 CPU

7.1.3 ROM

On the PCB, there is two sockets for installing ROMs, which is situated at the left middle of the PCB. IN TURBO XT, the leftmost is for installing BIOS using 2764, the other one is for installing BASIC ROM using 27256. In Turbo XT/2 and Turbo XT/3, both sockets are used for installing BIOS using 2764. Fig 7.4 shows the schematic circuit diagram of ROM in Turbo XT. Fig 7.5 shows the schematic circuit diagram of ROM in Turbo XT/2 and Turbo XT/3.

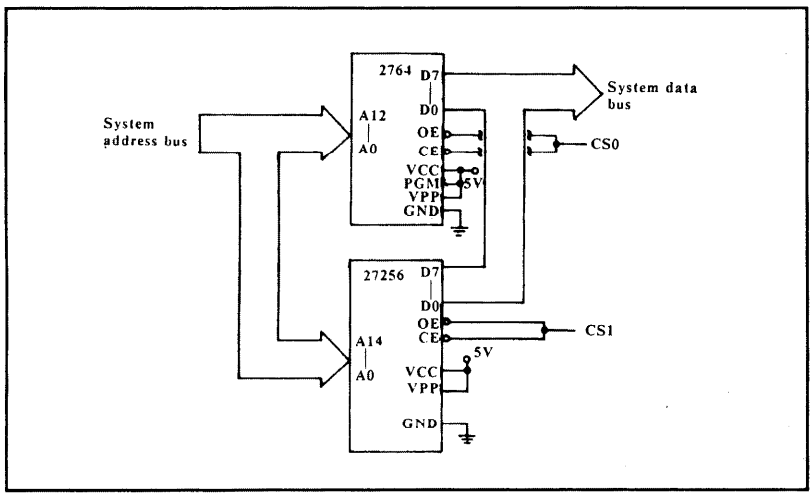


Fig 7.4 Schematic circuit diagram of ROM in Turbo XT

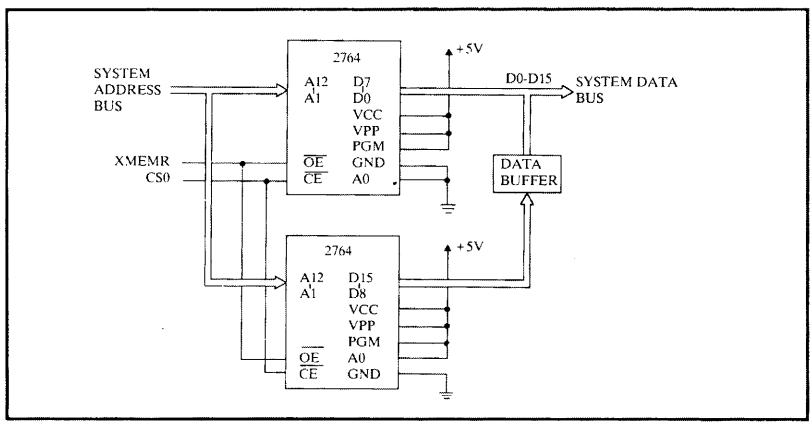


Fig 7.5 Schematic circuit diagram of ROM in Turbo XT/2 and Turbo XT/3.

The timing diagram of the ROM 2764 and 27256 is shown in Fig 7.6 and Fig 7.7 respectively.

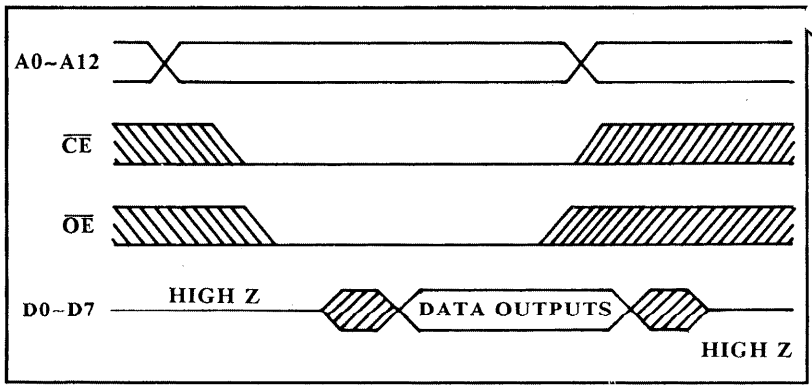


Fig 7.6 Timing diagram of 2764 ROM read

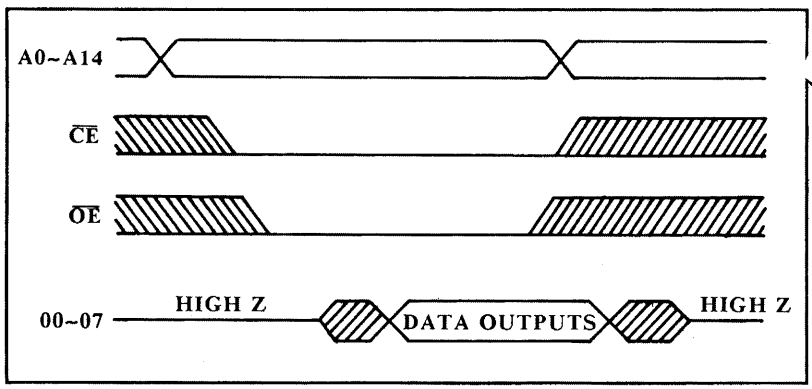


Fig 7.7 Timing diagram of 27256 ROM read

7.1.4 RAM

The computer can supports a maximum of 640K conventional memory and 1M expanded memory.

The 640K conventional memory have four rows of DRAM, the first two rows consists of two 4464 and one 4164. The second two rows consists of nine 41256. The Expanded Memory should be installed with 41256. The RAMs are accessed by the RAS and CAS signals which are obtained from the Gate Array A2 or A2.1.

7.1.5 Speaker circuit

The speaker should be connected to jumper J11. The Speaker circuit is shown in Fig 7.8.

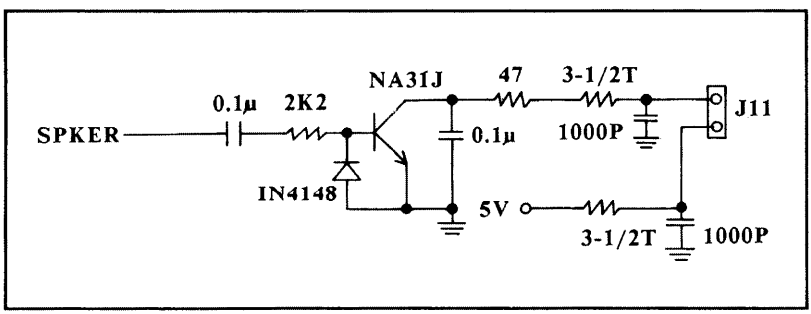


Fig 7.8 Speaker Circuit

7.1.6 Keyboard Lock and LED indicator

Jumper J12 is used for connecting Keyboard Lock, power indicator and High Speed indicator, the jumper should be connected as shown in Fig 7.9 on Turbo XT and Turbo XT/2.

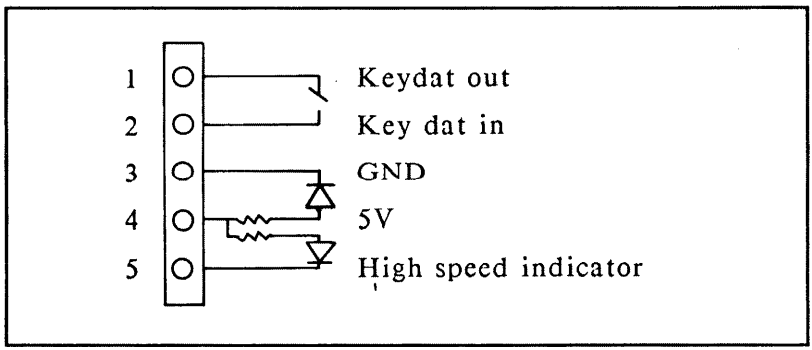


Fig 7.9 circuit of display panel for Turbo XT and Turbo XT/2.

For Turbo XT/3, a function panel is provided. There are two versions and their circuits are shown in Fig 7.10 and 7.11.

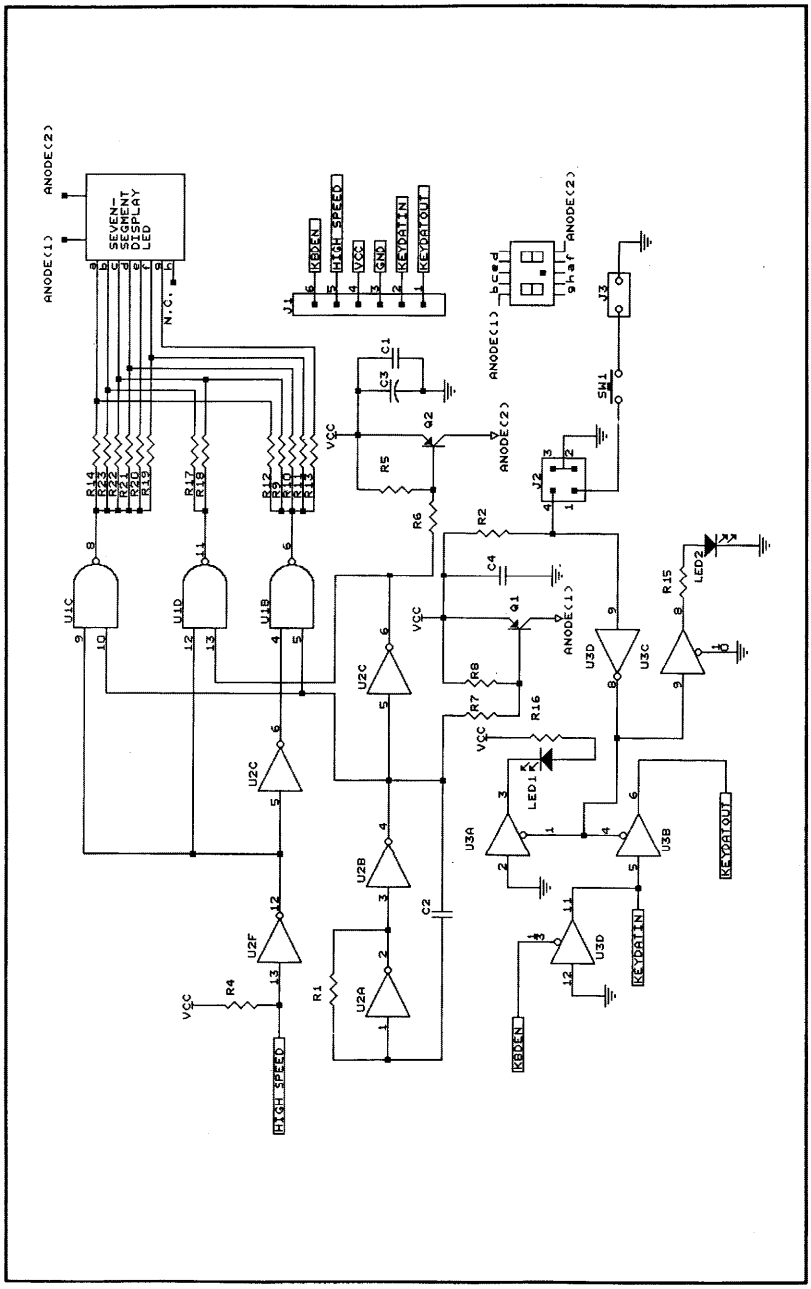


Fig 7.10 Circuits of display panel for Turbo XT/3 (Version 1)

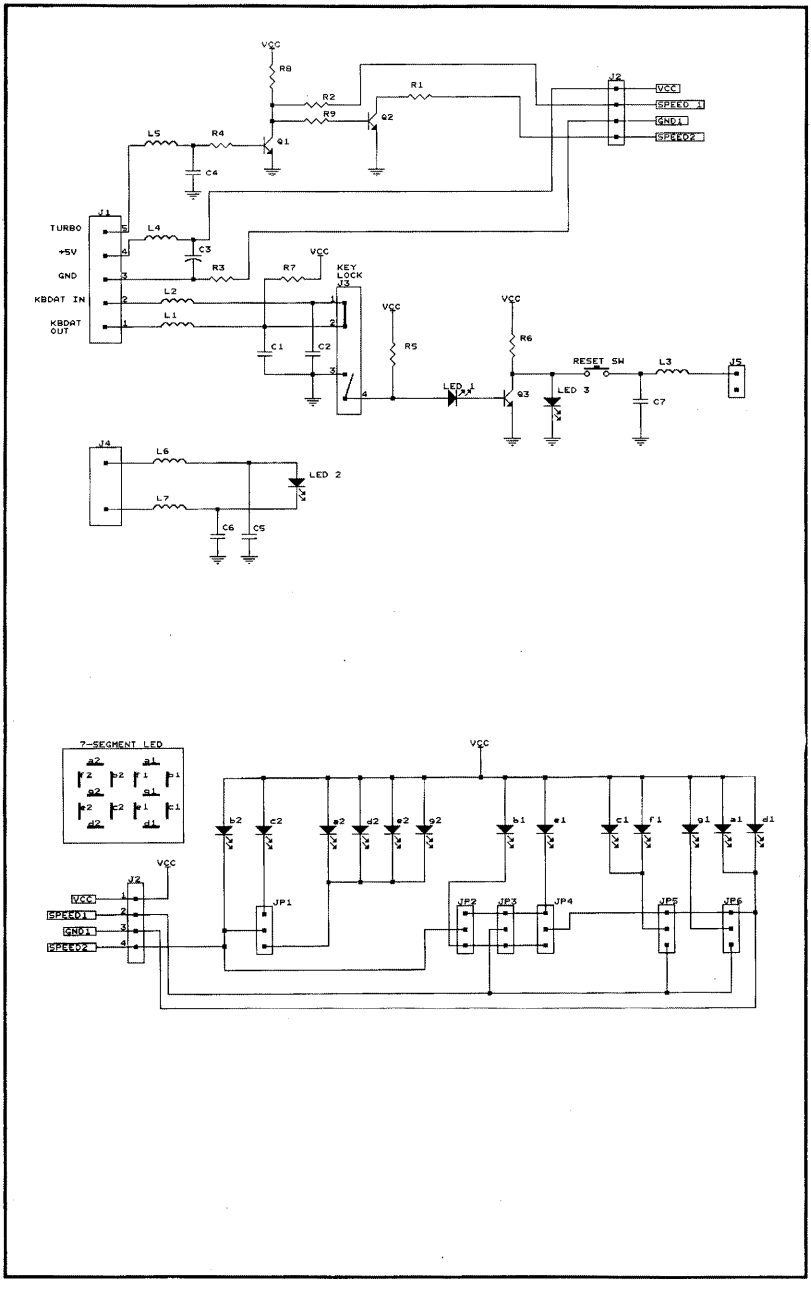
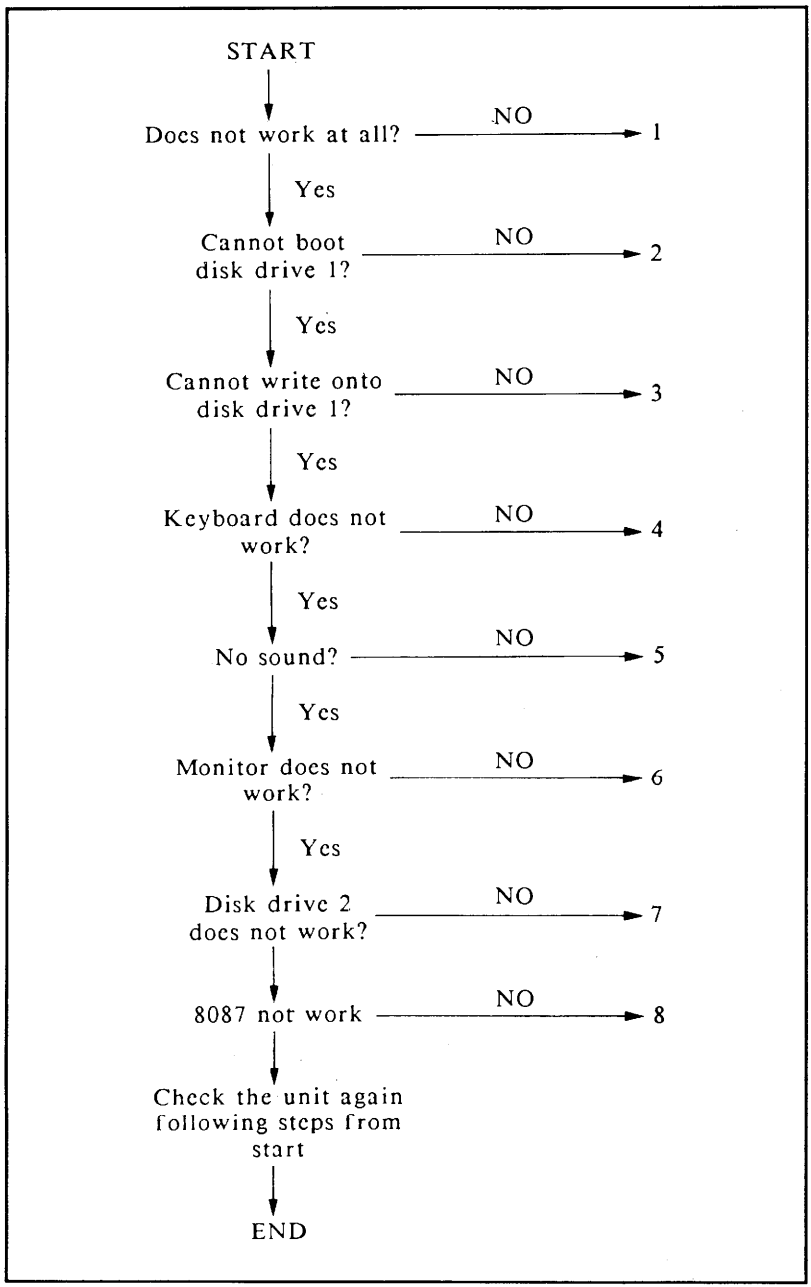
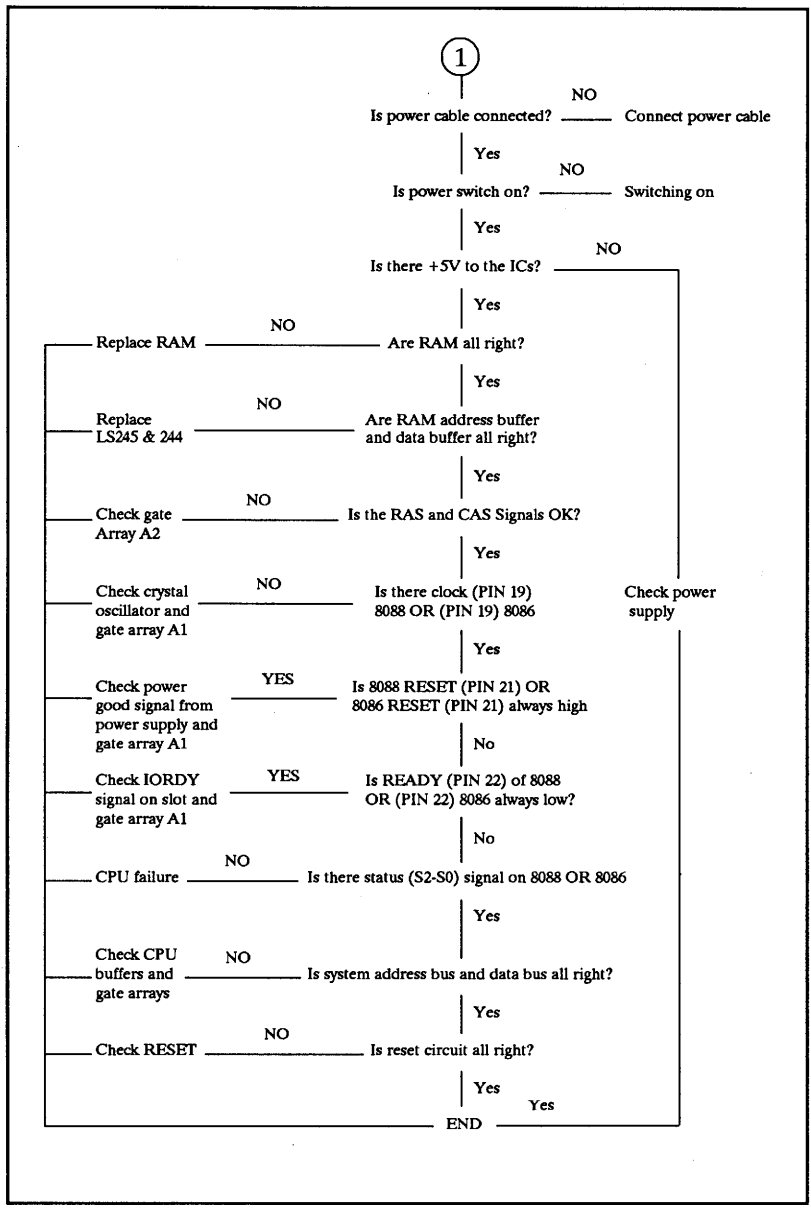
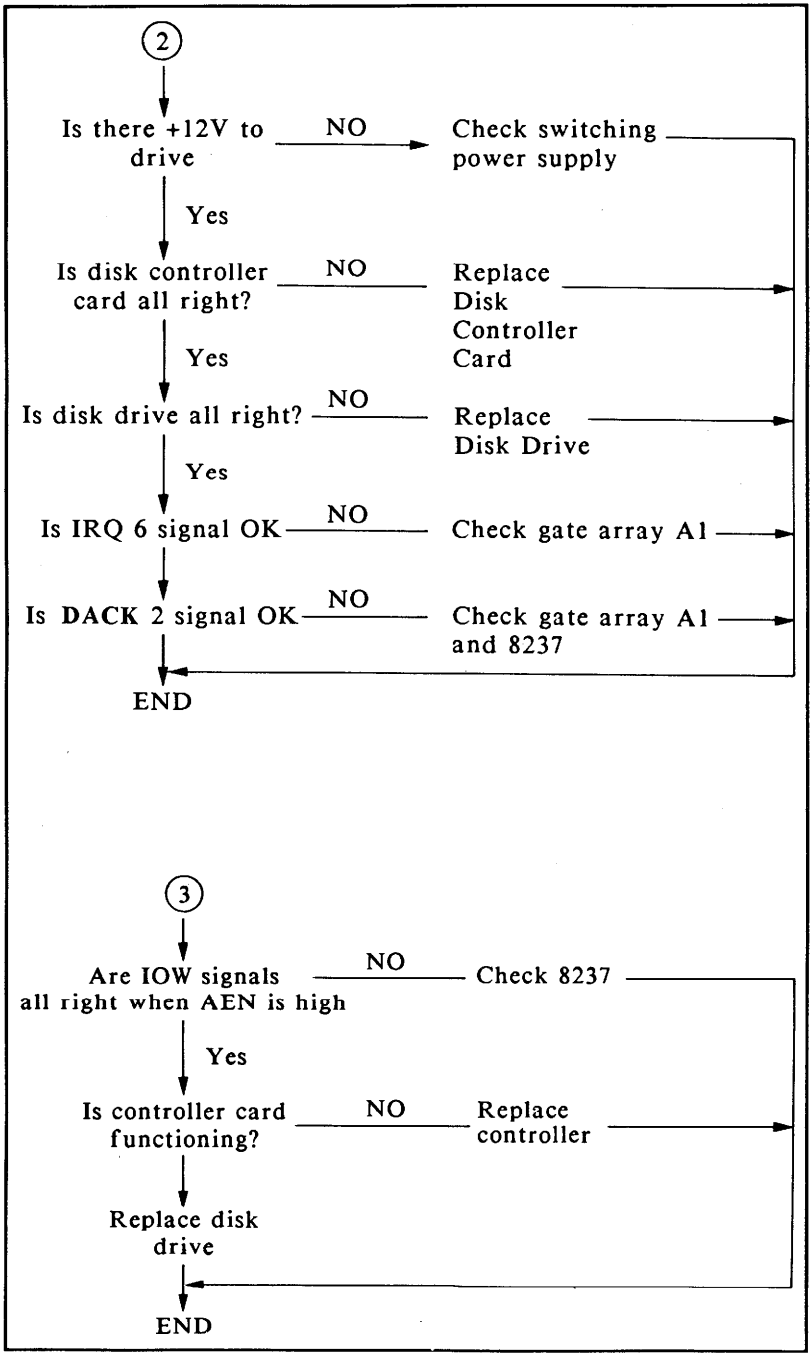


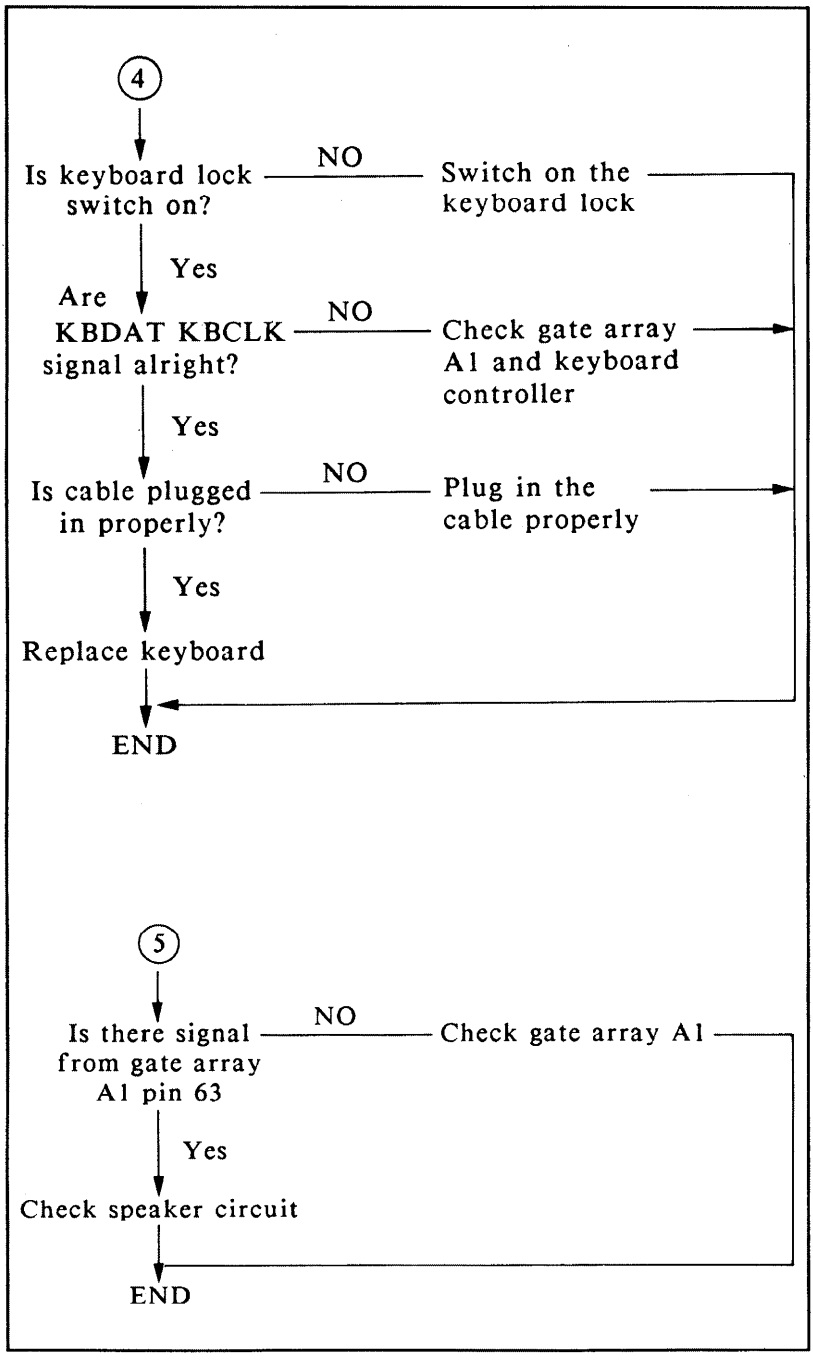
Fig 7.11 Circuits of display panel for Turbo XT/3 (Version 2)

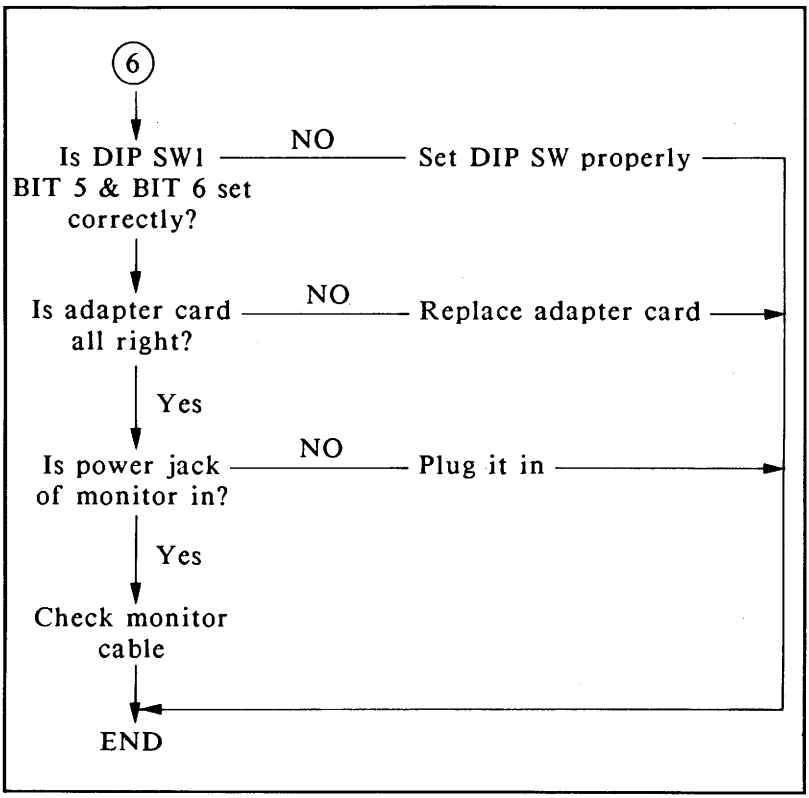
7.2 Service flow Chart

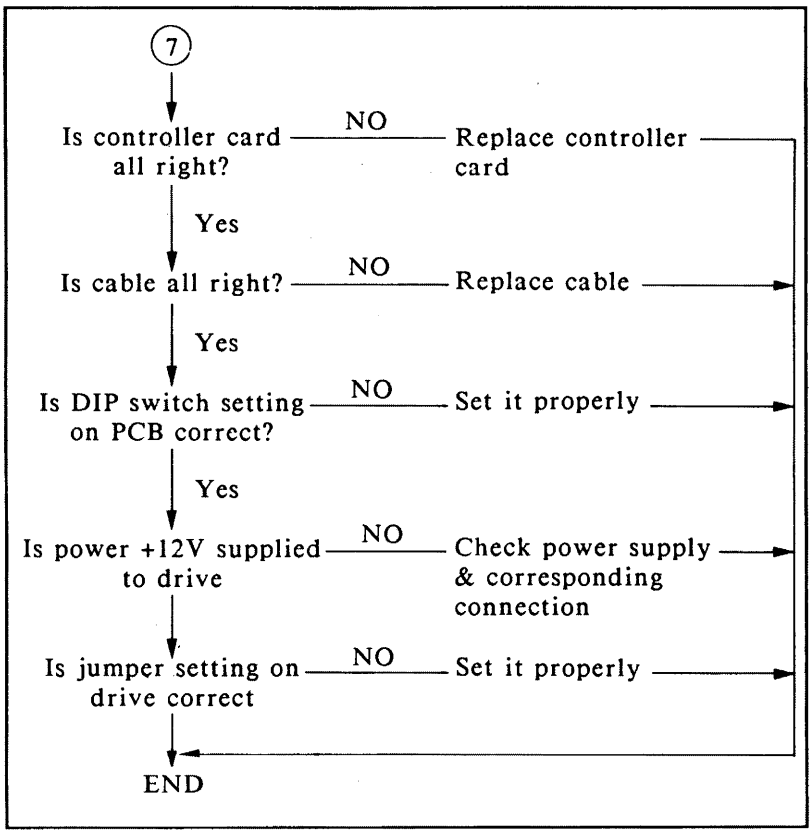


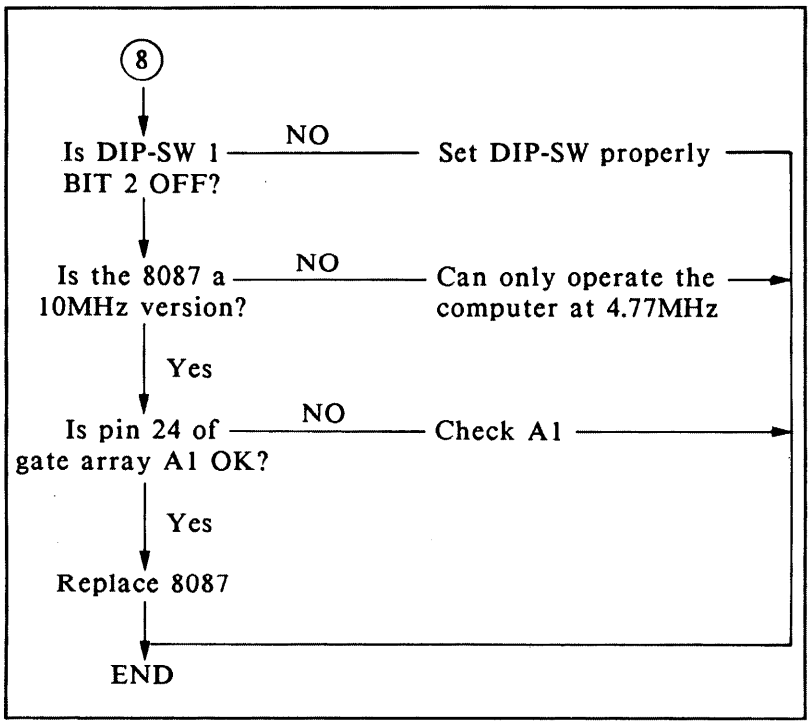

1
Is power cable connected?
NO
Connect power cable
Yes
Is power switch on?
NO
Switching on
Yes
Is there +5V to the ICs?
NO
Yes
Are RAM all right?
NO
Replace RAM
Yes
Are RAM address buffer and data buffer all right?
NO
Replace LS245 & 244
Yes
Is the RAS and CAS Signals OK?
NO
Check gate Array A2
Yes
Is there clock (PIN 19) 8088 OR (PIN 19) 8086
NO
Check crystal oscillator and gate array A1
Check power supply
Yes
Is 8088 RESET (PIN 21) OR 8086 RESET (PIN 21) always high
YES
Check power good signal from power supply and gate array A1
No
Is READY (PIN 22) of 8088 OR (PIN 22) 8086 always low?
YES
Check IORDY signal on slot and gate array A1
No
Is there status (S2-S0) signal on 8088 OR 8086
NO
CPU failure
Yes
Is system address bus and data bus all right?
NO
Check CPU buffers and gate arrays
Yes
Is reset circuit all right?
NO
Check RESET
Yes
END
Yes


2
Is there +12V to drive
NO
Check switching power supply
Yes
Is disk controller card all right?
NO
Replace Disk Controller Card
Yes
Is disk drive all right?
NO
Replace Disk Drive
Yes
Is IRQ 6 signal OK
NO
Check gate array A1
Is DACK 2 signal OK
NO
Check gate array A1 and 8237
END
3
Are IOW signals all right when AEN is high
NO
Check 8237
Yes
Is controller card functioning?
NO
Replace controller
Replace disk drive
END


4
Is keyboard lock switch on?
NO
Switch on the keyboard lock
Yes
Are KBDAT KBCLK signal alright?
NO
Check gate array A1 and keyboard controller
Yes
Is cable plugged in properly?
NO
Plug in the cable properly
Yes
Replace keyboard
END
5
Is there signal from gate array A1 pin 63
NO
Check gate array A1
Yes
Check speaker circuit
END


6
Is DIP SW1 BIT 5 & BIT 6 set correctly?
NO
Set DIP SW properly
Is adapter card all right?
NO
Replace adapter card
Yes
Is power jack of monitor in?
NO
Plug it in
Yes
Check monitor cable
END


7
Is controller card all right?
NO
Replace controller card
Yes
Is cable all right?
NO
Replace cable
Yes
Is DIP switch setting on PCB correct?
NO
Set it properly
Yes
Is power +12V supplied to drive
NO
Check power supply & corresponding connection
Is jumper setting on drive correct
NO
Set it properly
END


8
Is DIP-SW 1 BIT 2 OFF?
NO
Set DIP-SW properly
Is the 8087 a 10MHz version?
NO
Can only operate the computer at 4.77MHz
Yes
Is pin 24 of gate array A1 OK?
NO
Check A1
Yes
Replace 8087
END

APPENDIX A

GATE ARRAY A1 SPECIFICATION

APPENDIX A
GATE ARRAY A1 SPECIFICATION

A.1 A1 Functional Description

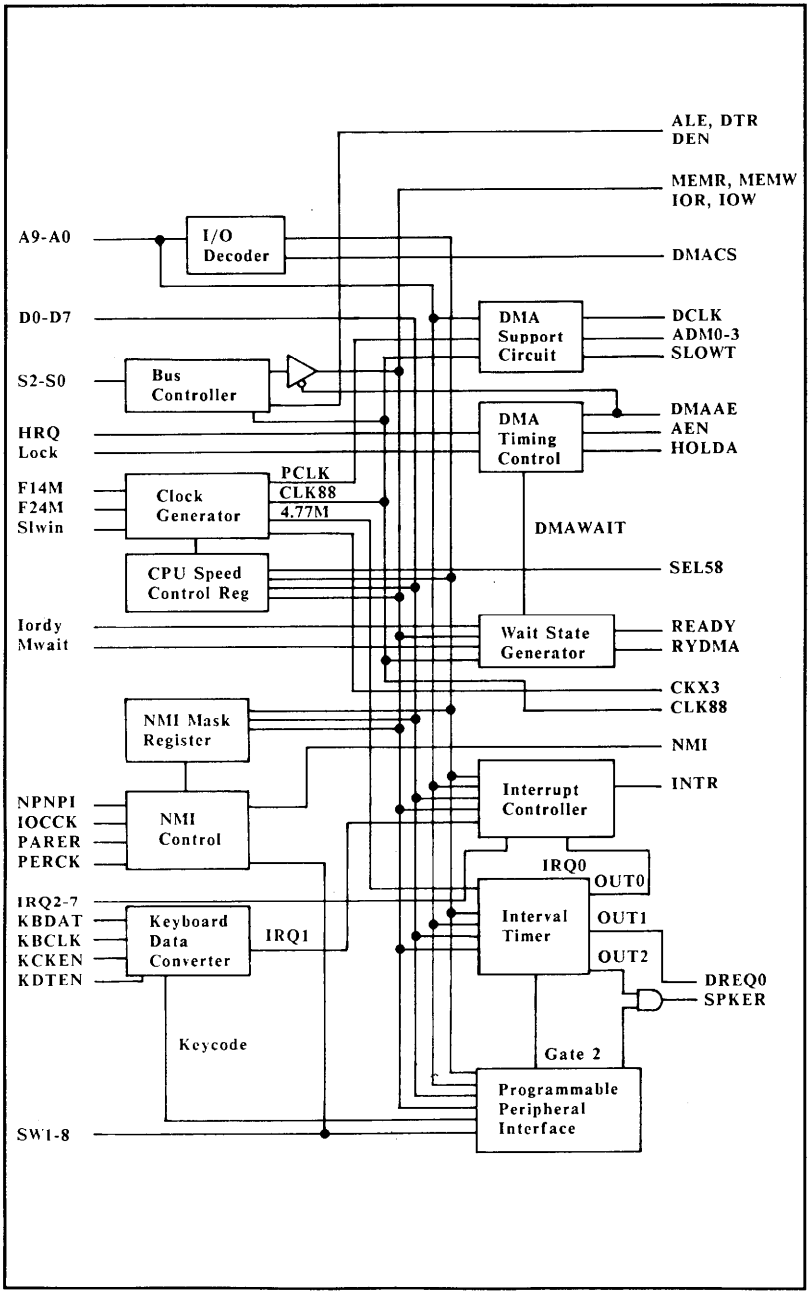
The gate array A1 is used to replaced most of the IBM PC/XT main board logics. It integrates the functions of the following chips:

8284A clock generator
8288 bus controller
8259A programmable interrupt controller
8253-5 programmable interval timer
8255A-5 programmable peripheral interface

In addition, it also incorporates the keyboard data converter, the wait state generator, DMA timing generator and I/O decoding circuitry.

The gate array A1 was designed to support high speed operation of the microprocessor. The processor can be switched to operate at the standard speed (4.77MHz) or higher speed through the control of software.

A.2 A1 FUNCTION DIAGRAM



A.3 Gate Array A1 Pin Usage

Pin No	Pin type	Name	Description
2	I	A9	CPU address line
3	I	A8	"
4	I	A7	"
5	I	A6	"
6	I	A5	"
7	I	A4	"
8	I	A3	"
9	I	A2	"
10	I	A1	"
11	I	A0	"
28	I/O	D7	CPU data line
29	I/O	D6	"
30	I/O	D5	"
31	I/O	D4	"
32	I/O	D3	"
33	I/O	D2	"
34	I/O	D1	"
35	I/O	D0	"

<table>
<tr><th>Pin No</th><th>Pin type</th><th>Name</th><th>Description</th></tr>
<tr><td>12</td><td>I</td><td>S2</td><td>Status Inputs from CPU.</td></tr>
<tr><td>13</td><td>I</td><td>S1</td><td>External pull up needed.</td></tr>
<tr><td>14</td><td>I</td><td>S0</td><td>
<table>
<tr><th>S2</th><th>S1</th><th>S0</th><th>Signal activated</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>INTA (internal signal)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>IOR</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>IOW</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>halt (no signal active)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>MEMR</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>MEMR</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>MEMW</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>no signal active</td></tr>
</table>
</td></tr>
<tr><td>16</td><td>I</td><td>LOCK</td><td>Lock signal from CPU.
Disable DMA operation when low.</td></tr>
<tr><td>17</td><td>I</td><td>F14M</td><td>14.31818 MHz clock input.
It is divided by 3 to obtain the CPU clock at standard speed.</td></tr>
<tr><td>18</td><td>I</td><td>F24M</td><td>High frequency clock input.
It is divided by 3 to obtain the CPU clock at high speed.</td></tr>
<tr><td>77</td><td>O</td><td>CKX3</td><td>Three times the frequency of CLK88.
Always synchronizes with CLK88.</td></tr>
<tr><td>19</td><td>O</td><td>CLK88</td><td>Clock for the CPU.
33% duty cycle.
4.77 M at standard speed.
At high speed mode equals to F24M divided by 3.</td></tr>
</table>

Pin No	Pin type	Name	Description
21	O	ALE	Address latch enable. (active high) This signal is used to strobe an address into the address latches during T1.
22	O	DEN	Data Enable. (active low, the corresponding signal of 8288 is active high) It is used to enable data onto either the local or system data bus.
23	O	DTR	Data Transmit/Receive It establishes the direction of data flow through the transceivers. A high indicates Transmit and a low indicates Receive.
39	I/O	MEMW	Memory Write, active low
40	I/O	MEMR	Memory Read, active low
42	I/O	IOW	I/O Write, active low
43	I/O	IOR	I/O read, active low These four signals will be tristated during DMA operation. During which these signals are asserted by the DMA controller. External pull up are needed.
26	O	READY	Ready signal to CPU. It is used to insert wait states to the CPU.

Pin No	Pin type	Name	Description
62	I	MWAIT	Memory Wait It serves to insert wait state to the CPU during memory read or write operation. A wait state is only insert under the following conditions: - the system is in high speed mode - MWAIT is high MWAIT must be stable throughout the period when MEMR or MEMW is active.
27	O	INTR	Interrupt Request to CPU
25	O	NMI	Non-maskable Interrupt request to CPU
24	I	NPNPI	Interrupt Request from the numeric proc essor. When this signal is active (high), a NMI will be initiated if the signal SW2 is also high.
44	I	IRQ7	Interrupt requests from peripherals.
45	I	IRQ6	They are prioritized with IRQ2 as
46	I	IRQ5	the highest priority and IRQ7 as
47	I	IRQ4	the lowest. An Interrupt is
48	I	IRQ3	generated by raising an IRQ line
38	I	IRQ2	(low to high) and holding it high until it is acknowledged by the CPU. These lines are pulled low internally.
1	I	IOCHK	I/O Channel Check When this input is low, a NMI will be initiated to the CPU.

Pin No	Pin	Name	Description
37	I	IORDY	I/O Channel Ready This line, normally high (ready), is pulled low to lengthen I/O or memory cycles. Any slow device using this line should drive it low immediately upon detecting a valid address and a Read or Write command.
60	I	EXRES	Active low reset input. Serves for power up reset. Internal Schmitt trigger input.
100	I	KYRES	Active low reset input. Serves for external hardware reset. Internal Schmitt trigger input.
49	O	SYRES	Active low reset output. It is synchronized with the falling edge of CLK88.
50	I	SW8	DIP Switch bit 8
51	I	SW7	DIP Switch bit 7
52	I	SW6	DIP Switch bit 6
53	I	SW5	DIP Switch bit 5
54	I	SW2	DIP Switch bit 2
55	I	SW1	DIP Switch bit 1
56	I/O	KBDAT	Keyboard data input. It will be forced low after receiving an keyboard code.

Pin No	Pin	Name	Description
57	I/O	KBCLK	Keyboard clock The keyboard data is strobed using the falling edge of the keyboard clock. Can be forced low through control of an internal register.
59	O	KDTEN	Keyboard data output enable A low indicates the KBDAT signal is in output mode.
58	O	KCKEN	Keyboard clock output enable. A low indicates the KBCLK signal is in output mode. Both KDTEN and KCKEN is used to control external buffers for the KBDAT and KBCLK signals when the loading is too high, otherwise they can be left un used.
61	I	PARER	Parity error input This is used to detect parity error of RAM. This pin should be tied to the PARER pin of gate array A2. If parity check is not needed, tied this pin to ground.
94	I	PERCK	Parity error clock This is used to strobe the PARER signal. Normally this pin should be tied to the MEMR signal.
66	O	DMACS	DMA controller chip select. active through the address range 000H-01FH.
67	O	RYDMA	Ready signal to the DMA controller

Pin No	Pin	Name	Description
68	O	DCLK	Clock output to the DMA controller
70	O	HOLDA	Hold acknowledge to the DMA controller. It is an active high signal indicating that the CPU has relinquished control of the bus.
71	I	HRQ	Hold Request from the DMA controller.
20	O	AEN	Address Enable When this line is active (high), the DMA controller has control of the address bus, data bus and read write command lines (IOR, IOW, MEMR, MEMW).
96	O	DMAAE	DMA address enable Active (low) during DMA operation. It serves to control address buffers of the DMA controller.
95	I	DACK0	DMA acknowledge 0
72	O	DREQ0	DMA request to the DMA controller channel 0. It is an active high signal which originates from channel 1 of the internal programmable interval timer. This signal is cleared when DACK0 is low. Normally DMA channel 0 serves the function of Dynamic RAM refreshing.
73	OZ	ADM0	To A0 of DMA controller.
74	OZ	ADM1	To A1 of DMA controller.
75	OZ	ADM2	To A2 of DMA controller.

Pin No	Pin	Name	Description
76	OZ	ADM3	To A3 of DMA controller. ADM0 - ADM3 will be tri-stated during DMA operation.
36	O	DIR	Direction control of external data buffer. For large system, the D7 - D0 needed be buffered by external transreceiver. When DIR is low, data is transferred from the A1 to external.
64	I	DCNT1	Data buffer control 1 If the data transreceiver is shared by the DMA controller, tied this pin to DMACS, otherwise to Vcc
79	I	DCNT2	Data buffer control 2 If the data transreceiver is shared by ROM 0, tied this pin to the CS0 signal of gate array A2, otherwise to Vcc
80	I	DCNT3	Data buffer control 3 If the data transreceiver is shared by ROM 1, tied this pin to the CS1 signal of gate array A2, otherwise to Vcc.
97	I	SLWIN	CPU speed select A high selects standard speed (CLK88 = 4.77MHz), a low selects high speed (CLK88 = F24M / 3). Normally this pin should be tied to SLOT.

Pin No	Pin	Name	Description
98	O	SLWOT	CPU speed control It serves to control the speed of the CPU. This signal will be low when switched to high speed mode. However, it will be forced high under the following condition: - when CPU is doing I/O operation. - when the system is doing DMA operation.
99	O	SEL58	CPU speed indication A high indicates high speed mode. A low indicates standard speed mode.
63	O	SPKER	Speaker output This signal should be connected to a driver circuit to sound a loudspeaker.
81	I	FRSTP	
82	I	RWSEK	
83	I	TRKO	
85	O	STEP	equals to FRSTP AND RWSEK
86	O	FTRK0	equals to RWSEK AND TRK0
78	I	VC0	
84	I	SEPDA	
87	O	RDDAT	equals to VC0 AND NOT SEPDA
88	I	BUFEN	
89	I	RTCEN	

Pin No	Pin	Name	Description
90	I	COMEN	
92	I	GRDEN	
93	O	PDIR	equals to (IOR AND IOW) OR (BUFEN AND RTCEN AND NOT COMEN AND GRDEN) This pins are garbage collector for peripherals. For normal design just tie the inputs to ground and left the outputs unused.
69	I	TEST	Test pin. Must tie it to ground.
15			GROUND
65			GROUND
41			Vcc
91			Vcc

A.4 GATE ARRAY A1 AC CHARACTERISTICS

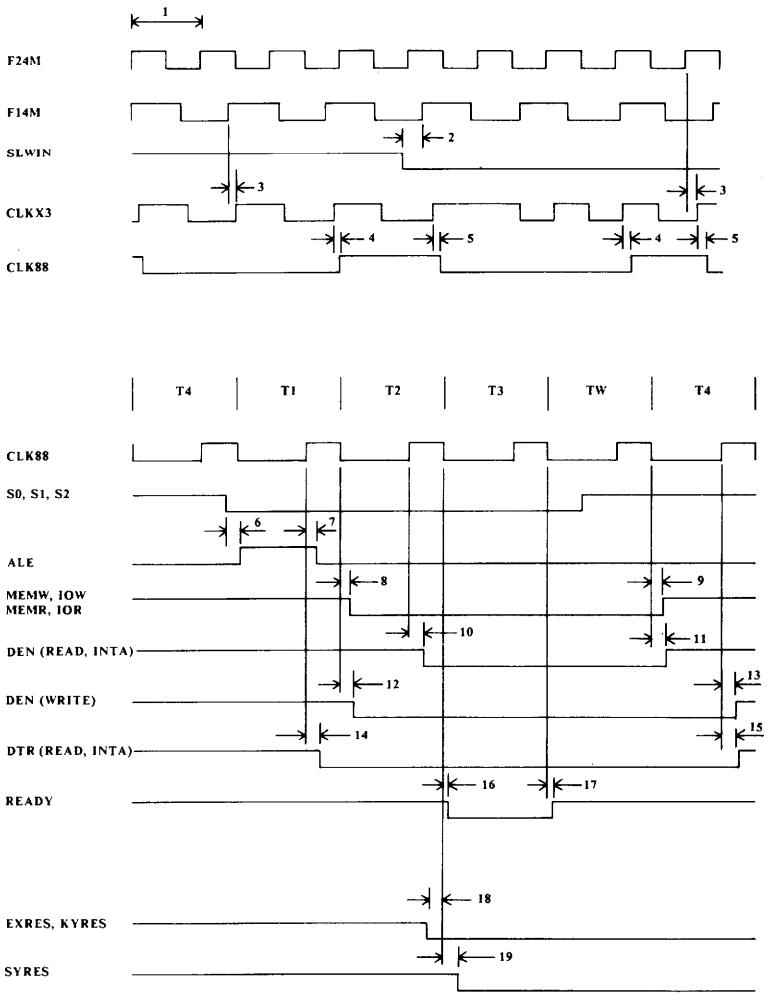
(Vcc = 5V +/-5%, Ta = 0 to 70 C, pin capacitive load = 50pF)

	Min. (ns)	Max (ns)
1. F24M period	27	
2. SLWIN set up time	10	
3. CLKX3 delay from F14M	9	44
4. CLK88 high from CLKX3	6	16
5. CLK88 low from CLKX3	7	20
6. ALE active from S0,S1,S2	7	35
7. ALE inactive delay	2	11
8. MEMW, IOW, MEMR, IOR active delay	4	21
9. MEMW, IOW, MEMR, IOR inactive delay	2	13
10. DEN active delay	3	22
11. DEN inactive delay	6	31
12. DEN active delay	7	31
13. DEN inactive delay	2	18
14. DTR active delay	3	19
15. DTR inactive delay	3	20
16. READY active delay	-3	4

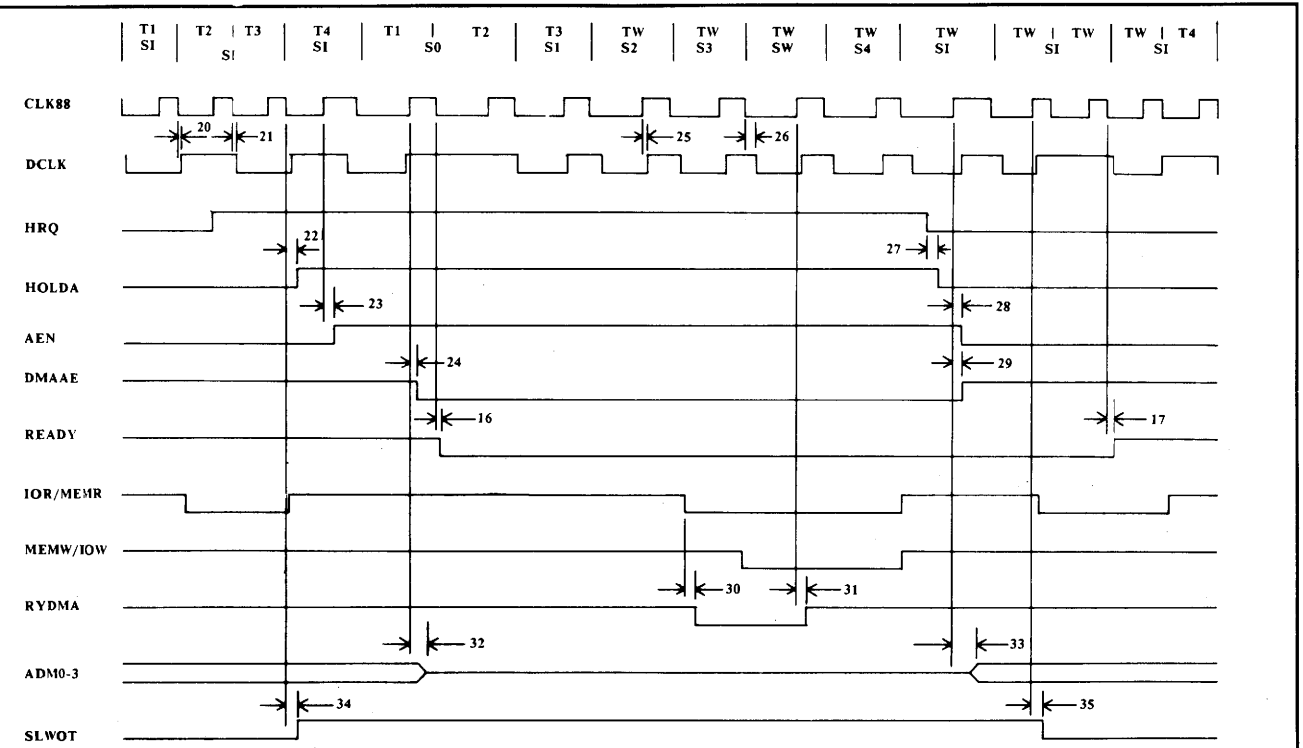
	Min. (ns)	Max (ns)
17. READY inactive delay	0	-10
18. EXRES,KYRES setup time	35	
19. SYRES delay	3	18
20. DCLK high delay (CLK88 / 2)	5	25
21. DCLK low delay (CLK88 / 2)	5	27
22. HOLDA delay	4	20
23. AEN active delay	2	10
24. DMAAE active delay	4	24
25. DCLK high delay (CLK88)	3	16
26. DCLK low delay (CLK88)	10	46
27. HOLDA inactive delay	9	45
28. AEN inactive delay	2	18
29. DMAAE inactive delay	2	17
30. RYDMA active delay	12	60
31. RYDMA inactive delay	2	16
32. ADM0-3 tristate delay	7	37
33. AMD0-3 active delay	7	37
34. SLWOT rising delay from CLK88	5	26

	Min. (ns)	Max (ns)
35. SLWOT falling delay from CLK88	4	24
36. SLWOT rising delay from IOR, IOW	8	39
37. SLWOT falling delay from IOR,IOW	8	40
38. MWAIT set up time	12	
39. MWAIT hold time	7	
40. IORDY active set up time	58	
41. IORDY inactive set up time	45	
42. DMACS active delay	10	52
43. DMACS inactive delay	7	37
44. NMI active delay from NPNPI	7	38
45. NMI inactive delay from NPNPI	8	44
46. Pulse width of IOCHK	20	
47. NMI active delay from IOCHK	9	47
48. NMI inactive delay from IOW	12	61
49. PARER to PERCK set up time	7	
50. NMI to PERCK delay	8	41
51. SEL58 delay from IOW	9	49

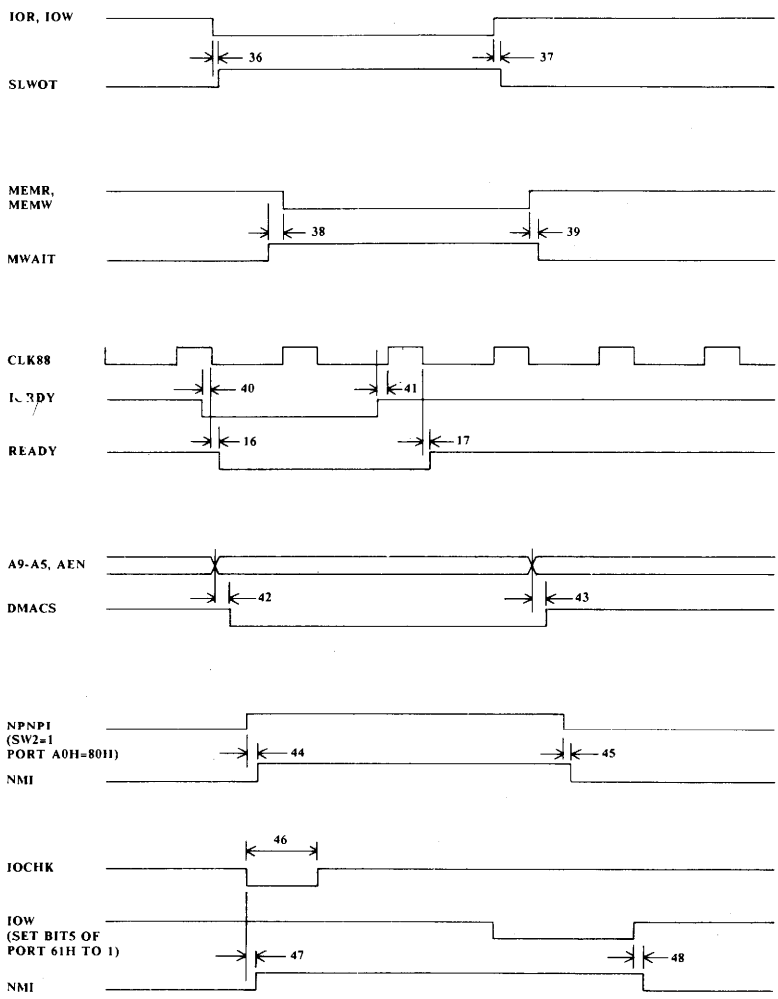
	Min. (ns)	Max (ns)
52. DREQ0 delay from DACK0	8	44
53. KBDAT to KBCLK set up time	-420	
54. KBDAT to KBCLK hold time	1260	
55. KDTEN, KCKEN delay from IOW	11	55
56. DIR active delay from DCNT2, DCNT3	8	39
57. DIR inactive delay from DCNT2, DCNT3	8	39
58. STEP delay from FRSTP, RWSEK	7	37
59. FTRK0 delay from RWSEK, TRK0	7	38
60. RDDAT delay from VC0, SEPDA	7	38
61. PDIR active delay from IOR, IOW	9	46
62. PDIR inactive delay from IOR, IOW	7	37
63. PDIR delay from BUFEN, RTCEN, COMEN, GRDEN	9	45

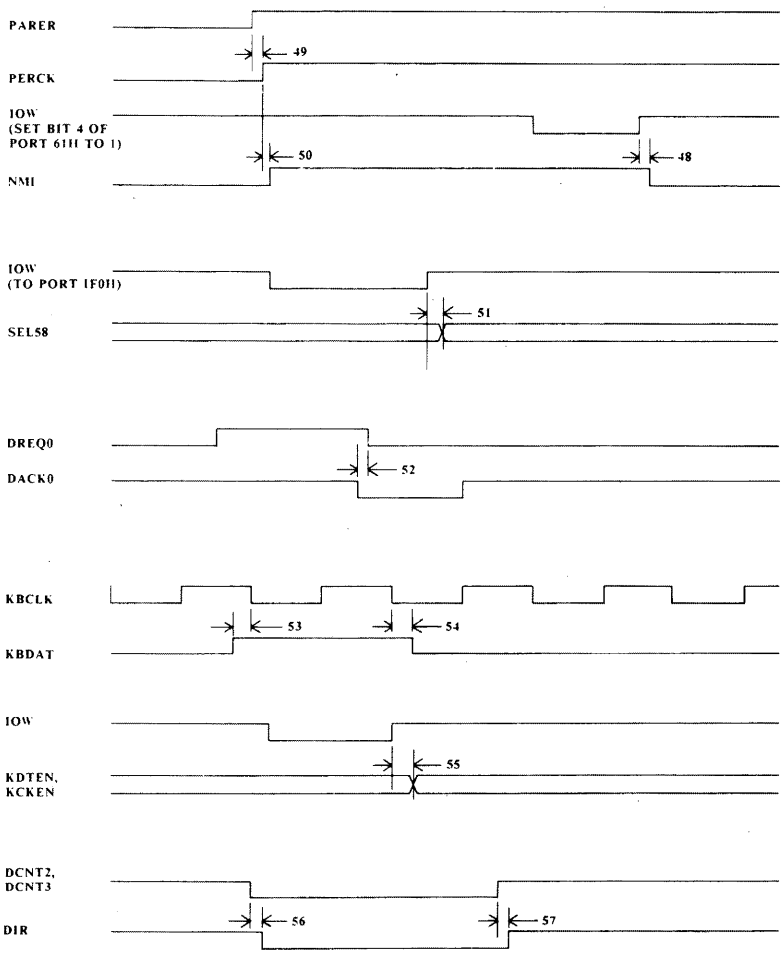


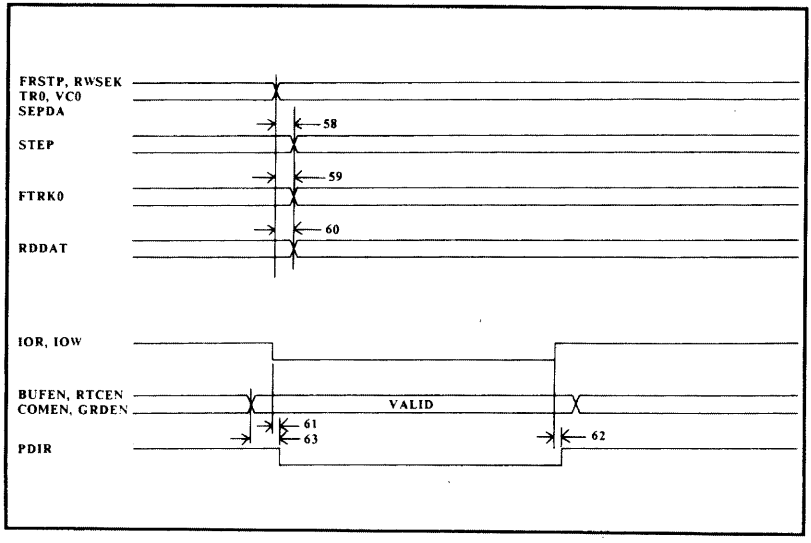
A1 TIMING DIAGRAM



AN EXAMPLE OF DMA TIMING AT HIGH SPEED MODE


IOR, IOW
SLWOT
36
37
MEMR,
MEMW
MWAIT
38
39
CLK88
IOCHRDY
READY
40
41
16
17
A9-A5, AEN
DMACS
42
43
NPNPI
(SW2=1
PORT A0H=80H)
NMI
44
45
46
IOCHK
IOW
(SET BIT5 OF
PORT 61H TO 1)
NMI
47
48


PARER
49
PERCK
IOW
(SET BIT 4 OF
PORT 61H TO 1)
50
48
NMI
IOW
(TO PORT 1F0H)
51
SEL58
DREQ0
52
DACK0
KBCLK
53
54
KBDAT
IOW
55
KDTEN,
KCKEN
DCNT2,
DCNT3
56
57
DIR


FRSTP, RWSEK
TR0, VC0
SEPDA
STEP
FTRK0
RDDAT
IOR, IOW
BUFEN, RTCEN
COMEN, GRDEN
PDIR
VALID
58
59
60
61
63
62

Appendix B

Gate array A2 specification

Gate array A2.1 specification

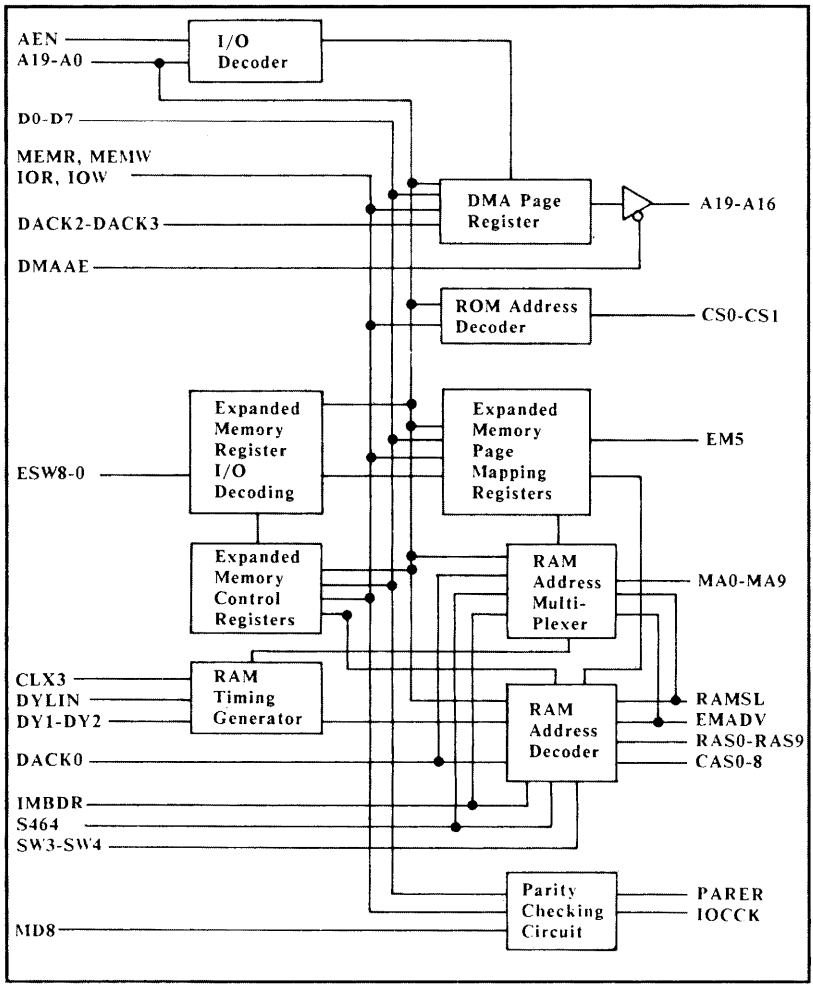
Appendix B
Gate array A2 specification

B.1 A2 functional description

The gate array A2 integrates the following functions:

Support system RAM up to 640K.
Support Expanded Memory which conforms to the Lotus®/Intel® Expanded memory standard. A maximum of 4 Mbyte can be added.
DRAM parity checking circuitry.
ROM address decoding.
DMA page register.

B.2 A2 Function diagram



B.3 Gate Array A2 pin usage

Pin No	Pin Type	Name	Description
71	I/O	A19	CPU address line
72	I/O	A18	"
73	I/O	A17	"
74	I/O	A16	" The contents of the DMA page register will be output on A19 - A16 during DMA operation
75	I	A15	CPU address line
76	I	A14	"
77	I	A13	"
78	I	A12	"
79	I	A11	"
80	I	A10	"
81	I	A9	"
82	I	A8	"
83	I	A7	"
84	I	A6	"
85	I	A5	"
86	I	A4	"
87	I	A3	"

Pin No	Pin Type	Name	Description
88	I	A2	"
89	I	A1	"
90	I	A0	"
62	I/O	D7	CPU data line
61	I/O	D6	"
60	I/O	D5	"
58	I/O	D4	"
56	I/O	D3	"
55	I/O	D2	"
57	I/O	D1	"
59	I/O	D0	"
96	I	IOR	I/O read.
95	I	IOW	I/O write.
94	I	MEMR	Memory read.
93	I	MEMW	Memory write.
42	I	RESET	This is an active low reset signal with schmit trigger input level.
40	I	DMAAE	DMA address enable Control output of A19 - A16, When it is low, contents of DMA page register will be output on A19-A16.

Pin No	Pin Type	Name	Description
70	I	AEN	address enable
99	I	DACK0	DMA acknowledge 0
100	I	DACK2	DMA acknowledge 2
98	I	DACK3	DMA acknowledge 3
45	I	SW3	DIP-SW 3
44	I	SW4	DIP-SW 4 SW3 and SW4 are used to select size of system RAM : SW4 SW3 Size of system RAM 0 0 256 K 0 1 512 K 1 0 576 K 1 1 640 K
52	I	ESW2	ESW2 - ESW0 are used to control
53	I	ESW1	I/O address of Expanded Memory
54	I	ESW0	board 0
49	I	ESW5	ESW5 - ESW3 are used to control
50	I	ESW4	I/O address of Expanded Memory
51	I	ESW3	board 1
46	I	ESW8	ESW8 - ESW6 are used to control
47	I	ESW7	I/O address of Expanded Memory
48	I	ESW6	board 2

Pin No	Pin Type	Name	Description
97	I/O	MD8	Memory Data Bit 8 It connects directly to bit 8 of DRAM to provide error detection.
34	O	PARER	Parity error output It is the output of the parity checking circuit. It should be connected to the PARER input of gate array A1.
69	OZ	IOCCK	I/O channel check This signal provides parity check for the Expanded Memory. A low indicates parity error. A subsequent memory write will reset it to normal state (tri-stated). System RAM parity error is NOT checked by this signal, so this pin is useful when the A2 is used alone on an Expanded Memory Card.
43	I	CLK88	System Clock input. It should be connected to the CPU clock.
39	I	CKX3	High frequency Clock input. This pin should be tied to a signal which is three times the frequency of CLK88 and synchronized with it. It is used to generated the RAS, CAS and multiplexed address timing.
66	I	DYLIN	Delay line select. When tied to high, all RAM timing will be controlled by an external delay line. For some applications the CKX3 signal is unavailable, then a delay line is necessary for providing RAS and CAS timing.

Pin No	Pin Type	Name	Description
63	I	DY2	When DYLIN is high, the RAM multiplexed addresses will be con trolled by this signal. A low selects column addresses.
64	I	DY1	When DYLIN is high, the CAS signal will be delayed by this signal.
35	O	CS0	ROM 0 Chip Select Memory address range : FE000H - FFFFFH
36	O	CS1	ROM 1 Chip Select Memory address range : F6000H - FDFFFH
10	O	RAS0	Row address strobe 0
11	O	RAS1	Row address strobe 1
12	O	RAS2	Row address strobe 2
13	O	RAS3	Row address strobe 3
14	O	RAS4	Row address strobe 4
16	O	RAS5	Row address strobe 5
17	O	RAS6	Row address strobe 6
18	O	RAS7	Row address strobe 7
19	O	RAS8	Row address strobe 8
20	O	RAS9	Row address strobe 9
9	O	CAS0	Column address strobe 0
8	O	CAS1	Column address strobe 1

Pin No	Pin Type	Name	Description
7	O	CAS2	Column address strobe 2
6	O	CAS3	Column address strobe 3
5	O	CAS4	Column address strobe 4
3	O	CAS5	Column address strobe 5
2	O	CAS6	Column address strobe 6
1	O	CAS7	Column address strobe 7
21	O	MA9	Multiplexed address for DRAM
22	O	MA8	"
32	O	MA8A	"
23	O	MA7	"
24	O	MA6	"
25	O	MA5	"
26	O	MA4	"
28	O	MA3	"
29	O	MA2	"
30	O	MA1	"
31	O	MA0	"
37	I	S464	Select 4464 Selects 4464 instead of 41256 as system RAM when this signal is high.

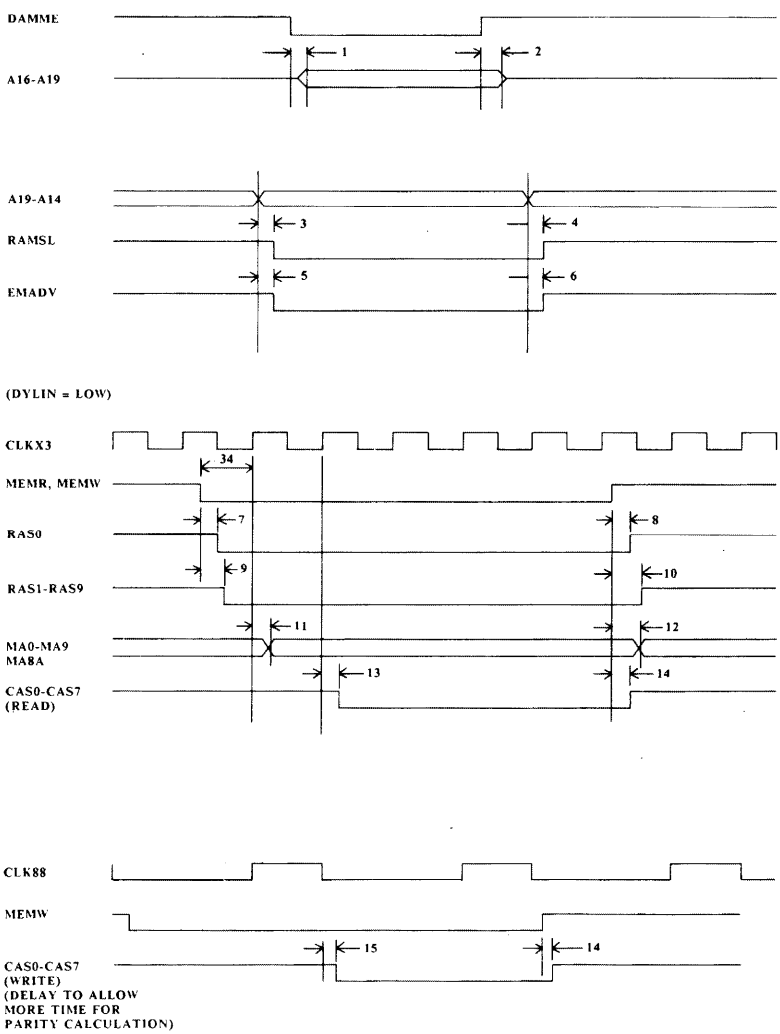
Pin No	Pin Type	Name	Description
38	I	IMBDR	Select 1 Mbit DRAM When this signal is high, 1 Mbit DRAM can be used to provide 640K of system memory, the remaining 384K is used as Expanded Memory.
67	O	DIR	Direction control for data transreceiver. For large system, D0-D7 needed be buffered by data transreceiver. A low of DIR indicates data to be read from A2 or the RAM. The data buffer is shared by A2 and the RAM.
68	O	RAMSL	RAM select A low indicates RAM (both system and expanded RAM) is being accessed by the CPU.
92	O	EMADV	Expanded Memory address Valid A low indicates Expanded Memory is being accessed by the CPU.
33	O	EM5	Expanded memory page register Bit 5. When the expanded memory is being accessed by the CPU, bit 5 of the active page register is output on this pin (but inverted). If the expanded memory is imple mented using 41256, then this signal can be used with A9 to decode four CAS signals.
4			Not used
27			Not used
15			Ground
65			Ground
41			Vcc
91			Vcc

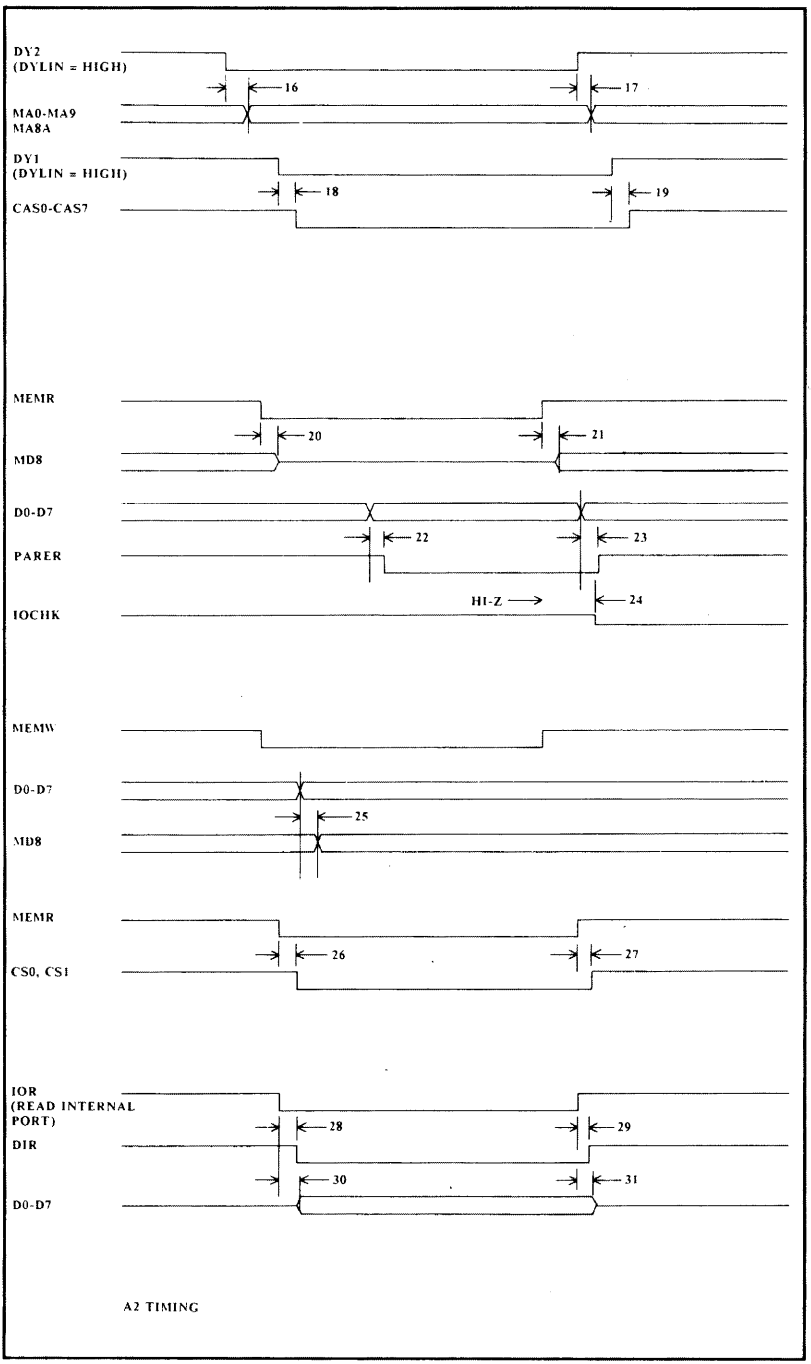
B.4 GATE ARRAY A2 AC CHARACTERISTICS

(Vcc = 5V +/-5%, Ta = 0 TO 70 C, pin capacitive load = 50pF)

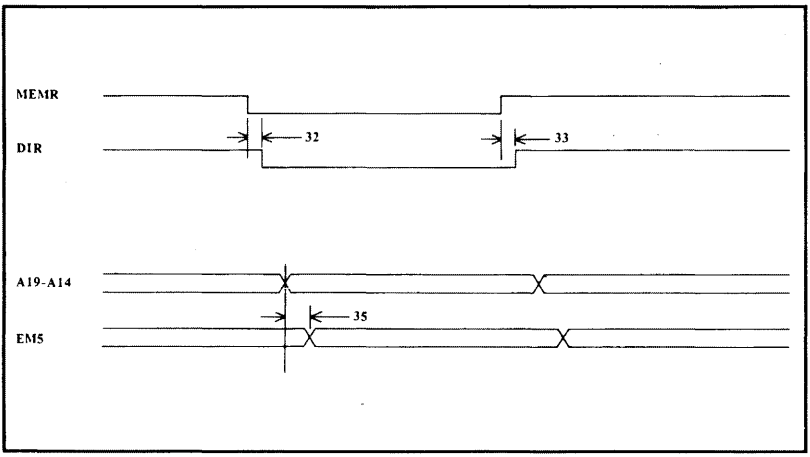
		Min (ns)	Max (ns)
1.	A19-A16 active delay	9	41
2.	A19-A16 inactive delay	7	33
3.	RAMSL active delay	14	63
4.	RAMSL inactive delay	14	61
5.	EMADV active delay	12	54
6.	EMADV inactive delay	11	50
7.	RAS0 active delay	8	38
8.	RAS0 inactive delay	7	30
9.	RAS1-RAS9 active delay	10	45
10.	RAS1-RAS9 inactive delay	10	45
11.	MA0-MA9 delay from CLKX3	9	44
12.	MA0-MA9 delay from MEMR	10	50
13.	CAS0-CAS7 delay from CLKX3	12	55
14.	CAS0-CAS7 delay from MEMR	9	43
15.	CAS0-CAS7 delay from CLK88	10	48
16.	MA0-MA9 delay from DY2	10	45
17.	MA0-MA9 delay from DY2	10	46

		Min (ns)	Max (ns)
18.	CAS0-CAS7 active delay from DY1	12	53
19.	CAS0-CAS7 inactive delay from DY1	9	40
20.	MD8 tri-state delay	8	39
21.	MD8 active delay from MEMR	9	45
22.	PARER active delay	10	50
23.	PARER inactive delay	10	45
24.	IOCHK active delay	9	47
25.	MD8 active delay from data	11	51
26.	CS0-CS1 active delay MEMR	10	50
27.	CS0-CS1 inactive delay from MEMR	8	35
28.	DIR active delay from IOR	9	44
29.	DIR inactive delay from IOR	8	37
30.	D0-D7 active delay	11	55
31.	D0-D7 tri-state delay	11	47
32.	DIR active delay from MEMR	10	44
33.	DIR inactive delay from MEMR	8	36
34.	MEMR and MEMW to CLKX3 set up time	15	
35.	EM5 delay	20	93


DAMME
A16-A19
1
2
A19-A14
RAMSL
EMADV
3
4
5
6
(DYLIN = LOW)
CLKX3
MEMR, MEMW
RAS0
RAS1-RAS9
MA0-MA9
MA8A
CAS0-CAS7
(READ)
34
7
8
9
10
11
12
13
14
CLK88
MEMW
CAS0-CAS7
(WRITE)
(DELAY TO ALLOW
MORE TIME FOR
PARITY CALCULATION)
15
14


DY2
(DYLIN = HIGH)
16
17
MA0-MA9
MA8A
DY1
(DYLIN = HIGH)
18
19
CAS0-CAS7
MEMR
20
21
MD8
D0-D7
22
23
PARER
HI-Z
24
IOCHK
MEMW
D0-D7
25
MD8
MEMR
26
27
CS0, CS1
IOR
(READ INTERNAL
PORT)
28
29
DIR
30
31
D0-D7

A2 TIMING


MEMR
DIR
32
33
A19-A14
EM5
35

Gate array A2.1 specification

B.5 A2.1 Functional Description

The gate array A2.1 operates in two modes. In one mode it supports the 8088 CPU. In the other mode it supports the 8086. A dedicated pin MODE86 (pin 37) is used to select the two modes.

In 8088 mode (MODE86 = ground), the gate array A2.1 integrates the following functions:

- Support system RAM up to 640K.
- Support Expanded Memory which conforms to the Lotus /Intel Expanded memory standard. A maximum of 4 Mbyte can be added.
- DRAM parity checking circuitry.
- ROM address decoding.
- DMA page register.

In 8086 mode (MODE86 = Vcc), the gate array A2.1 integrates the following functions:

- Support system RAM up to 736 K.
- Support Expanded Memory which conforms to the Lotus®/Intel® Expanded memory standard. A maximum of 1408 Kbyte can be added.
- 16 bit to 8 bit bus conversion.
- DRAM parity checking circuitry.
- ROM address decoding.
- DMA page register.

B.6. A2.1 Pin Description

The usage of pins are different in the two modes. So their usages will be described in two sections.

6.1 Pin usage in 8088 mode (MODE86 = ground)

Pin No	Pin Type	Name	Description
71	I/O	A19	CPU address line
72	I/O	A18	"
73	I/O	A17	"
74	I/O	A16	" The contents of the DMA page register will be output on A19 - A16 during DMA operation
75	I	A15	CPU address line
76	I	A14	"
77	I	A13	"
78	I	A12	"
79	I	A11	"
80	I	A10	"
81	I	A9	"
82	I	A8	"
83	I	A7	"

Pin No	Pin Type	Name	Description
84	I	A6	"
85	I	A5	"
86	I	A4	"
87	I	A3	"
88	I	A2	"
89	I	A1	"
90	I	A0	"
62	I/O	D7	CPU data line
61	I/O	D6	"
60	I/O	D5	"
58	I/O	D4	"
56	I/O	D3	"
55	I/O	D2	"
57	I/O	D1	"
59	I/O	D0	"
96	I	IOR	I/O read.
95	I	IOW	I/O write.

<table>
<tr><th>Pin No</th><th>Pin Type</th><th>Name</th><th>Description</th></tr>
<tr><td>94</td><td>I</td><td>MEMR</td><td>Memory read.</td></tr>
<tr><td>93</td><td>I</td><td>MEMW</td><td>Memory write.</td></tr>
<tr><td>42</td><td>I</td><td>RESET</td><td>This is an active low reset signal with schmitt trigger input level.</td></tr>
<tr><td>40</td><td>I</td><td>DMAAE</td><td>DMA address enable
Control output of A19 - A16, When it is low, contents of DMA page register will be output on A19-A16.</td></tr>
<tr><td>70</td><td>I</td><td>AEN</td><td>address enable</td></tr>
<tr><td>99</td><td>I</td><td>DACK0</td><td>DMA acknowledge 0</td></tr>
<tr><td>100</td><td>I</td><td>DACK2</td><td>DMA acknowledge 2</td></tr>
<tr><td>98</td><td>I</td><td>DACK3</td><td>DMA acknowledge 3</td></tr>
<tr><td>45</td><td>I</td><td>SW3</td><td>DIP-SW 3</td></tr>
<tr><td>44</td><td>I</td><td>SW4</td><td>DIP-SW 4
SW3 and SW4 are used to select size of system RAM :
<table>
<tr><th>SW4</th><th>SW3</th><th>Size of system RAM</th></tr>
<tr><td>0</td><td>0</td><td>256 K</td></tr>
<tr><td>0</td><td>1</td><td>512 K</td></tr>
<tr><td>1</td><td>0</td><td>576 K</td></tr>
<tr><td>1</td><td>1</td><td>640 K</td></tr>
</table>
These two pins are internally pulled high.</td></tr>
</table>

Pin No	Pin Type	Name	Description
52 53 54	I I I	ESW2 ESW1 ESW0	ESW2 - ESW0 are used to control I/O address of Expanded Memory board 0
49 50 51	I I I	ESW5 ESW4 ESW3	ESW5 - ESW3 are used to control I/O address of Expanded Memory board 1
46 47 48	I I I	ESW8 ESW7 ESW6	ESW8 - ESW6 are used to control I/O address of Expanded Memory board 2
97	I/O	MD8	Memory Data Bit 8 It connects directly to bit 8 of DRAM to provide error detection.
34	O	PARER	Parity error output It is the output of the parity checking circuit. It should be connected to the PARER input of gate array A1.
69	OZ	IOCCK	I/O channel check This signal provides parity check for the Expanded Memory. A low indicates parity error. A subsequent memory write will reset it to normal state (tri-stated). System RAM parity error is NOT checked by this signal, so this pin is useful when the A2.1 is used alone on an Expanded Memory Card.
43	I	CLK88	System Clock input. It should be connected to the CPU clock.

Pin No	Pin Type	Name	Description
39	I	CKX3	High frequency Clock input. This pin should be tied to a signal which is three times the frequency of CLK88 and syn chronized with it. It is used to generated the RAS, CAS and multiplexed address timing.
66	I	DYLIN	Delay line select. When tied to high, all RAM timing will be controlled by an external delay line. For some applications the CKX3 signal is unavailable, then a delay line is necessary for providing RAS and CAS timing.
63	I	DY2	When DYLIN is high, the RAM multiplexed addresses will be controlled by this signal. A low selects column addresses.
64	I	DY1	When DYLIN is high, the CAS signal will be delayed by this signal.
35	O	CS0	ROM 0 Chip Select Memory address range : FE000H - FFFFFH
36	O	Cs1	ROM 1 Chip Select Memory address range : F6000H - FDFFFH
10	O	RAS0	Row address strobe 0
11	O	RAS1	Row address strobe 1
12	O	RAS2	Row address strobe 2
13	O	RAS3	Row address strobe 3

Pin No	Pin Type	Name	Description
14	O	RAS4	Row address strobe 4
16	I/O	RAS5	Row address strobe 5 During reset, this pin is configured as input and an external pull up or down resistor should be used to set the value of an internal latch called S464. The latch is used to deter mine the usage of the pins RAS7 and RAS8.
17	O	RAS6	Row address strobe 6
18	O	RAS7	Row address strobe 7 If S464=0, output =RAS7. If S464=1, output =ROM address Select (FC000H-FFFFFH)
19	O	RAS8	Row address strobe 8 If S464=0, output = RAS8. If S464=1, output = ROM address Select (F8000H-FFFFFH)
20	O	RAS9	Row address strobe 9
9	O	CAS0	Column address strobe 0
8	O	CAS1	Column address strobe 1
7	O	CAS2	Column address strobe 2
6	O	CAS3	Column address strobe 3
5	O	CAS4	Column address strobe 4
3	O	CAS5	Column address strobe 5
2	O	CAS6	Column address strobe 6

Pin No	Pin Type	Name	Description
1	O	CAS7	Column address strobe 7
21	O	MA9	Multiplexed address for DRAM
22	O	MA8	"
32	O	MA8A	"
23	O	MA7	"
24	O	MA6	"
25	O	MA5	"
26	O	MA4	"
28	O	MA3	"
29	O	MA2	"
30	O	MA1	"
31	O	MA0	"
37	I	MODE86	Select 8086 mode If 0, select 8088 mode. If 1, select 8086 mode.
38	I	IMBDR	Select 1 Mbit DRAM When this signal is high, 1 Mbit DRAM can be used to provide 640K of system memory, the remaining 384K is used as Expanded Memory.

Pin No	Pin Type	Name	Description
67	O	DIR	Direction control for data transreceiver. For large system, D0-D7 needed be buff ered by data transceiver. A low of DIR indicates data to be read from A2.1 or the RAM. The data buffer is shared by A2.1 and the RAM.
68	O	RAMSL	RAM select A low indicates RAM (both system and expanded RAM) is being accessed by the CPU.
92	O	EMADV	Expanded Memory address Valid A low indicates Expanded Memory is being accessed by the CPU.
33	O	EM5	Expanded memory page register Bit 5. When the expanded memory is being accessed by the CPU, bit 5 of the active page register is output on this pin (but inverted). If the expanded memory is implemented using 41256, then this signal can be used with A9 to decode four CAS signals.
4			Not used
27			Not used
15			Ground
65			Ground
41			Vcc
91			Vcc

6.2 Pin usage in 8086 mode (MODE86 = Vcc)

Pin No	Pin Type	Name	Description
71	I/O	A19	CPU address line
72	I/O	A18	"
73	I/O	A17	"
74	I/O	A16	" The contents of the DMA page register will be output on A19 - A16 during DMA operation
75	I	A15	CPU address line
76	I	A14	"
77	I	A13	"
78	I	A12	"
79	I	A11	"
80	I	A10	"
81	I	A9	"
82	I	A8	"
83	I	A7	"
84	I	A6	"
85	I	A5	"

Pin No	Pin Type	Name	Description
86	I	A4	"
87	I	A3	"
88	I	A2	"
89	I	A1	"
90	I	DMAA0	Connect to address bus bit 0 of DMA con troller.
69	I	BHE	Bus high enable
64	I	AD0	Address data bus 0 Connect to AD0 of 8086
17	O	CONA0	A0 output to be used by 8 bit devices.
53	I/O	D15	CPU data line
52	I/O	D14	"
51	I/O	D13	"
49	I/O	D12	"
47	I/O	D11	"
46	I/O	D10	"
48	I/O	D9	"
50	I/O	D8	"
62	I/O	D7	"

Pin No	Pin Type	Name	Description
61	I/O	D6	"
60	I/O	D5	"
58	I/O	D4	"
56	I/O	D3	"
55	I/O	D2	"
57	I/O	D1	"
59	I/O	D0	"
96	I	IOR	I/O read.
95	I	IOW	I/O write.
94	I	MEMR	Memory read.
93	I	MEMW	Memory write.
42	I	RESET	This is an active low reset signal with schmitt trigger input level.
40	I	DMAAE	DMA address enable
40	I	DMAAE	Data enable Control output of A19 - A16, When it is low, contents of DMA page register will be output on A19-A16.
70	I	AEN	address enable
99	I	DACK0	DMA acknowledge 0

<table>
<tr><th>Pin No</th><th>Pin Type</th><th>Name</th><th>Description</th></tr>
<tr><td>100</td><td>I</td><td>DACK2</td><td>DMA acknowledge 2</td></tr>
<tr><td>98</td><td>I</td><td>DACK3</td><td>DMA acknowledge 3</td></tr>
<tr><td>18</td><td>I</td><td>DEN</td><td>Data enable
Connects to the bus controller.</td></tr>
<tr><td>19</td><td>I</td><td>DTR</td><td>Data Transmit/Receive
connects to the bus controller.</td></tr>
<tr><td>54</td><td>O</td><td>OEH</td><td>Output enable control of the data buffer D8-D15.</td></tr>
<tr><td>38</td><td>I</td><td>ALE</td><td>Address latch enable
connects to the bus controller.</td></tr>
<tr><td>45</td><td>I</td><td>SW3</td><td>DIP-SW 3</td></tr>
<tr><td>44</td><td>I</td><td>SW4</td><td>DIP-SW 4
SW3 and SW4 are used to select size of system RAM :
<table><tr><th>SW4</th><th>SW3</th><th>Size of system RAM</th></tr><tr><td>0</td><td>0</td><td>512 K</td></tr><tr><td>0</td><td>1</td><td>640 K</td></tr><tr><td>1</td><td>0</td><td>704 K</td></tr><tr><td>1</td><td>1</td><td>736 K</td></tr></table>These two pins are internally pulled high.</td></tr>
</table>

Pin No	Pin Type	Name	Description
97	I/O	MD8	Memory Data Bit 8 It connects directly to bit 8 of DRAM to provide error detection for D0 to D7.
63	I/O	MD16	Memory Data Bit 16 It connects directly to bit 16 of DRAM to provide error detection for D8 to D15.
34	I/O	PARERESW0	Parity error output It is the output of the parity checking circuit. It should be con nected to the PARER input of gate array A1. During reset, this pin is configured as input to read in the signal ESW0.
43	I	CLK88	System Clock input. It should be connected to the CPU clock.
39	I	CKX3	High frequency Clock input. This pin should be tied to a signal which is three times the frequency of CLK88 and synchronized with it. It is used to generated the RAS, CAS and multiplexed address timing.
66	I	F30M	28.63636 Mhz input
14	O	F14M	14.31818 Mhz output

<table>
<tr><th>Pin No</th><th>Pin Type</th><th>Name</th><th>Description</th></tr>
<tr><td>35</td><td>I/O</td><td>CS0ESW1</td><td>ROM 0 Chip Select
The address range is determined by two signal EN128 and EN256.
<table><tr><th>EN128</th><th>EN256</th><th>Memory address range</th></tr><tr><td>0</td><td>0</td><td>FE000H- FFFFFH</td></tr><tr><td>1</td><td>0</td><td>FC000H - FFFFFH</td></tr><tr><td>1</td><td>1</td><td>F8000H - FFFFFH</td></tr></table>During reset, this pin is configured as input to read in the signal ESW1.</td></tr>
<tr><td>36</td><td>I/O</td><td>CS1EN256</td><td>ROM 1 Chip Select
The address range is determined by two signal EN128 and EN256.
<table><tr><th>EN128</th><th>EN256</th><th>Memory address range</th></tr><tr><td>0</td><td>0</td><td>F6000H - FFFFFH</td></tr><tr><td>1</td><td>0</td><td>FC000H - FFFFFH</td></tr><tr><td>1</td><td>1</td><td>F8000H - FFFFFH</td></tr></table>When EN128 = 1, CS1 is ORed with MEMR.
During reset, this pin is configured as input to read in the signal EN256.</td></tr>
<tr><td>10</td><td>I</td><td>MWAIT</td><td>If high, one wait state will be in serted for memory access.</td></tr>
</table>

Pin No	Pin Type	Name	Description
21	I/O	IORDYEMS	This signal is used to insert wait states during 16 bit to 8 bit conversion. During reset, this pin is configured as input to read in the signal ESW2.
32	I	IORDYIN	I/O Channel Ready input connects to the I/O READY signals on the I/O slots.
11	O	RAS1	Row address strobe 1
12	O	RAS2	Row address strobe 2
20	O	RAS9	Row address strobe 9
13	O	SLOW	This signal will become high under the following conditions: - 16 bit to 8 bit conversion - accessing memory on the I/O slot. i.e. not accessing internal RAM or ROM. This pin can be used to slow down the clock rate of the CPU.
16	O	CMDLY	Command Delay This signal will become low under the following condition: - SEL58 is low. - AEN is high. - IOR or IOW is low. - MEMR or MEMW is low and not accessing internal RAM or ROM This pin can be used to enable the IOR, IOW, MEMR and MEMW signals for the I/O slot.

Pin No	Pin Type	Name	Description
33	I	SEL58	At high speed mode this pin should be tied high. At normal speed this pin should below.
9	O	CAS0L	Column address strobe 0 low
8	O	CAS0H	Column address strobe 0 high
7	O	CAS1L	Column address strobe 1 how
6	O	CAS1H	Column address strobe 1 high
5	O	CAS4L	Column address strobe 4 low
3	O	CAS4H	Column address strobe 4 high
2	O	CAS5L	Column address strobe 5 low
1	O	CAS5H	Column address strobe 5 high
22	O	MA8	Multiplexed address for DRAM
23	O	MA7	"
24	O	MA6	"
25	O	MA5	"
26	O	MA4	"
28	O	MA3	"
29	O	MA2	"
30	O	MA1	"
31	O	MA0	"

Pin No	Pin Type	Name	Description
37	I	MODE86	Select 8086 mode If 0, select 8088 mode. If 1, select 8086 mode.
67	I/O	DIREN128	Direction control for data transre ceiver. For large system, D8-D15 needed be buffered by data transreceiver. A low of DIREN128 indicates data to be read from A2.1 or the RAM. The data buffer is shared by A2.1 and the RAM. During reset, this pin is configured as input to read in the signal EN128.
68	I/O	T16N	A low indicates 16 bit to 8 bit conver sion is occuring. During reset, this pin is configured as input to read in the signal ENSYSEMS.
92	O	T4	A high signals the end of the first bus cycle during a 16 bit to 8 bit conver sion.
4			Not used
27			Not used
15			Ground
65			Ground
41			Vcc
91			Vcc

B.7. Electrical specifications

7.1 Absolute Maximum ratings

Parameter	Symbol	Rating	Unit
Supply voltage	Vcc	-0.3~+6.7	V
Terminal voltage	Vt	-0.3~Vcc+0.3	V
Output Current			
- per one output	Io	-8~+8	mA
- total	Iot	-40~+40	mA
Operating Temperature	Topr	-20~+75	C
Storage Temperature			
- with Bias	Tbias	-20~+85	C
- without Bias	Tstg	-55~+125	C

7.2 Electrical characteristics

Vcc=5V +/-5%, Ta = -20 to 75

Parameter	Symbol	Min	Max	unit
Input Voltage	VIH	2.2	Vcc+0.3	V
	VIL	-0.3	0.8	V
Output Voltage	VOH (IOH = -2 mA)	3.5		V
	VOL (IOL = 5 mA)		0.5	V
Input Leakage Current	ILI		1	uA
Output Leakage Current	ILO		1	uA

APPENDIX C

8086/8088 INSTRUCTION SET

APPENDIX C
8086/8088 INSTRUCTION SET

Mnemonic	Full Name
AAA	ASCII adjust for addition
AAD	ASCII adjust for division
AAM	ASCII adjust for multiplication
AAS	ASCII adjust for subtraction
ADC	Add with carry
ADD	Add
AND	AND
CALL	CALL
CBW	Convert byte to word
CLC	Clear carry flag
CLD	Clear direction flag
CLI	Clear interrupt flag
CMC	Complement carry flag
CMP	Compare
CMPS	Compare byte or word (of string)
CMPSB	Compare byte string
CMPSW	Compare word string
CWD	Convert word to double word
DAA	Decimal adjust for addition
DAS	Decimal adjust for subtraction
DEC	Decrement
DIV	Divide
ESC	Escape
HLT	Halt
IDIV	Integer divide
IMUL	Integer multiply
IN	Input byte or word
INC	Increment
INT	Interrupt
INTO	Interrupt on overflow
IRET	Interrupt return
JA	Jump on above
JAE	Jump on above or equal
JB	Jump on below
JBE	Jump on below or equal

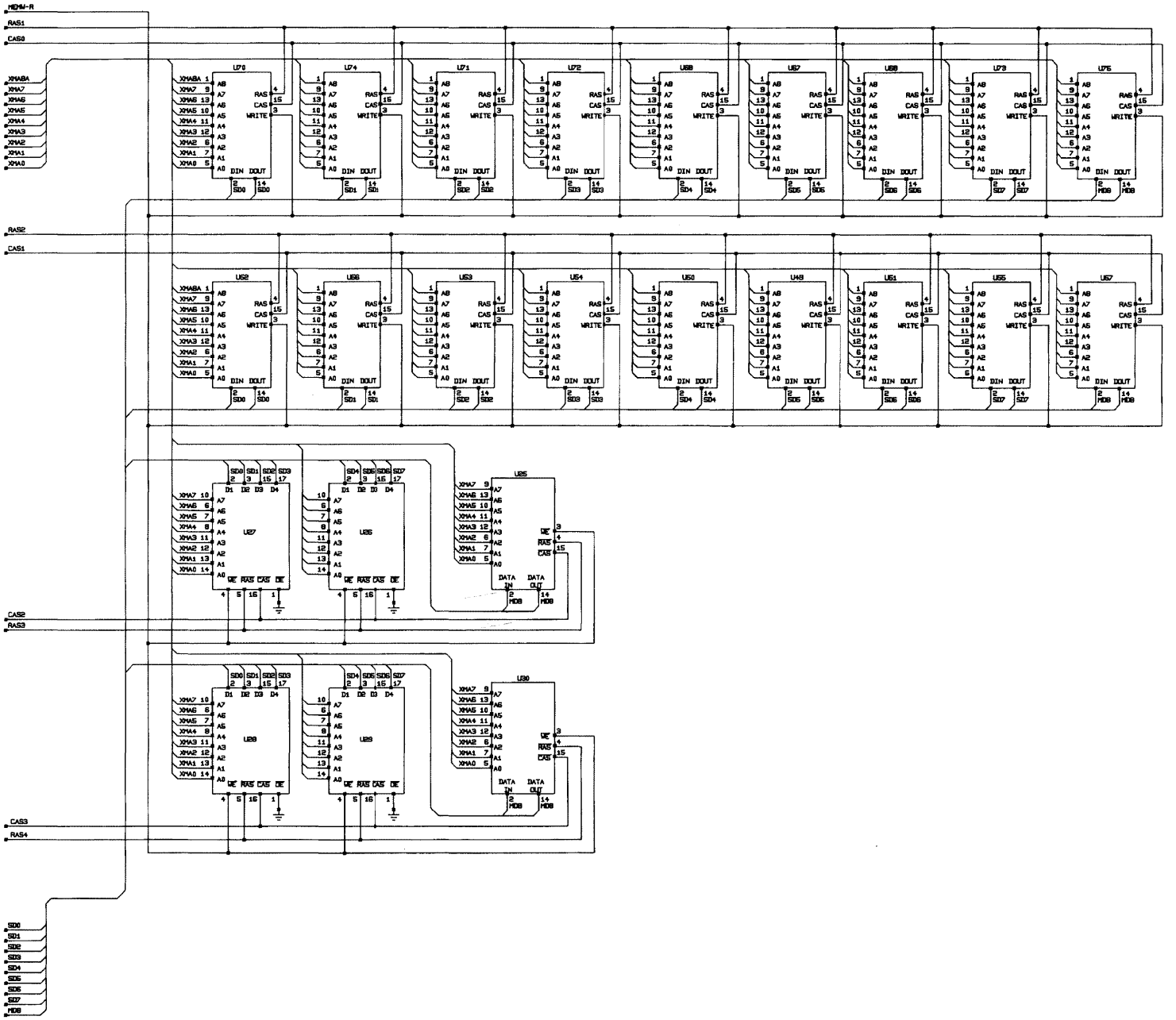
Mnemonic	Full Name
JC	Jump on carry
JCXC	Jump on CX zero
JE	Jump on equal
JG	Jump on greater
JGE	Jump on greater or equal
JL	Jump on less than
JLE	Jump on less than or equal
JMP	Jump
JNA	Jump on not above.
JNAE	Jump on not above or equal
JNB	Jump on not below
JNBE	Jump on not below or equal
JNC	Jump on no carry
JNE	Jump on not equal
JNG	Jump on not greater
JNGE	Jump on not greater or equal
JNL	Jump on not less than
JNLE	Jump on not less than or equal
JNO	Jump on not overflow
JNP	Jump on not parity
JNS	Jump on not sign
JNZ	Jump on not zero
JO	Jump on overflow
JP	Jump on parity
JPE	Jump on parity even
JPO	Jump on parity odd
JS	Jump on sign
JZ	Jump on zero
LAHF	Load AH with flags
LDS	Load pointer into DS
LEA	Load effective address
LES	Load pointer into ES
LOCK	LOCK bus
LODS	Load byte or word (of string)
LODSB	Load byte (string)
LODSW	Load word (string)
LOOP	LOOP
LOOPE	LOOP while equal

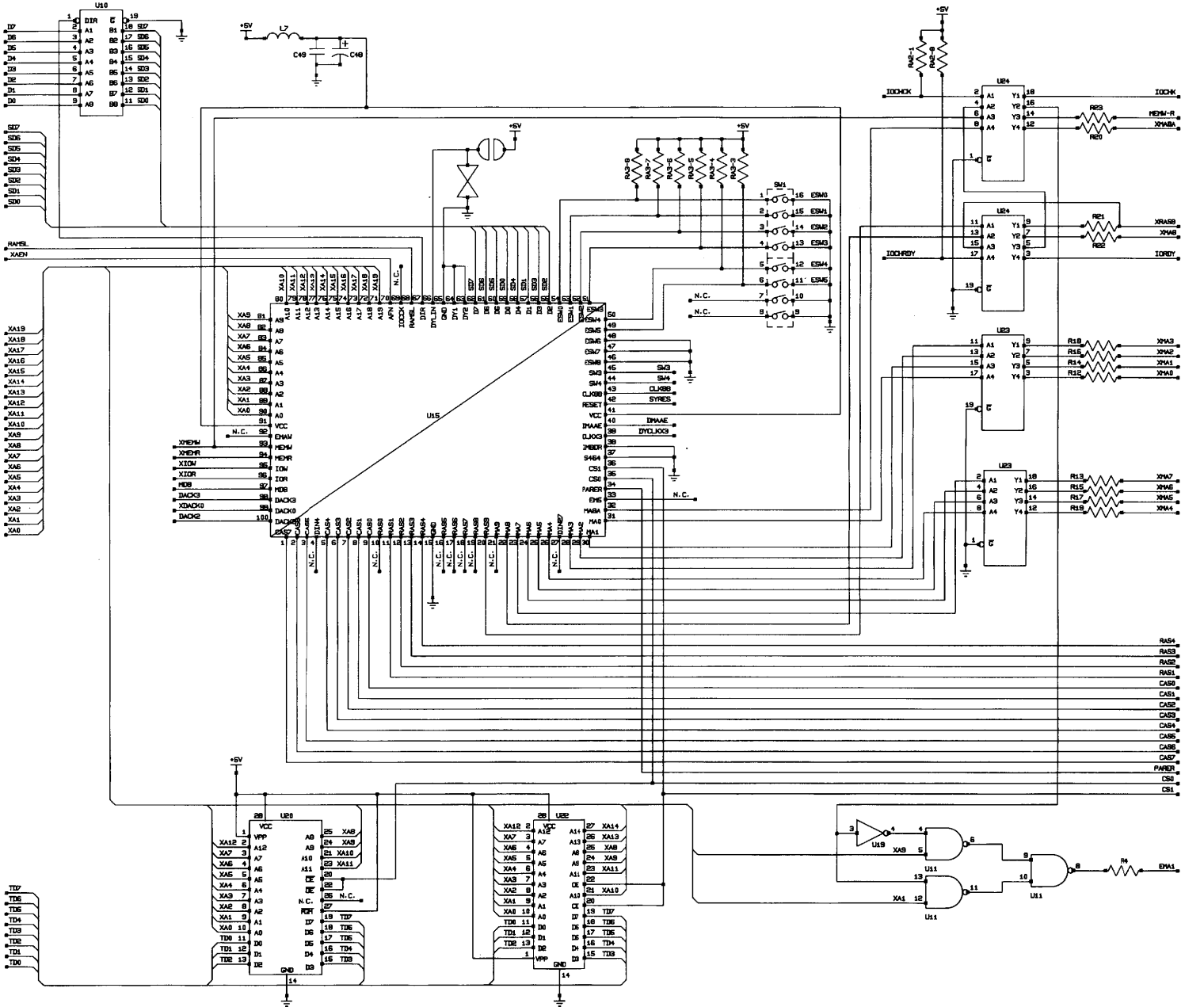
Mnemonic	Full Name
LOOPNE	LOOP while not equal
LOOPNZ	LOOP while not zero
LOOPZ	LOOP while zero
MOV	Move
MOVS	Move byte or word (of string)
MOVSB	Move byte (string)
MOVSW	Move word (string)
MUL	Multiply
NEG	Negate
NOP	No operation
NOT	NOT
OR	OR
OUT	Output byte or word
POP	POP
POPF	POP flags
PUSH	PUSH
PUSHF	PUSH flags
RCL	Rotate through carry left
RCR	Rotate through carry right
REP	Repeat
RET	Return
ROL	Rotate left
ROR	Rotate right
SAHF	Store AH into flags
SAL	Shift arithmetic left
SAR	Shift arithmetic right
SBB	Subtract with borrow
SCAS	Scan byte or word (of string)
SCASB	Scan byte (string)
SCASW	Scan word (string)
SHL	Shift left
SHR	Shift right
STC	Set carry flag
STD	Set direction flag
STI	Set interrupt flag
STOS	Store byte or word (of string)
STOSB	Store byte (string)
STOSW	Store word (string)
SUB	Subtract
TEST	TEST

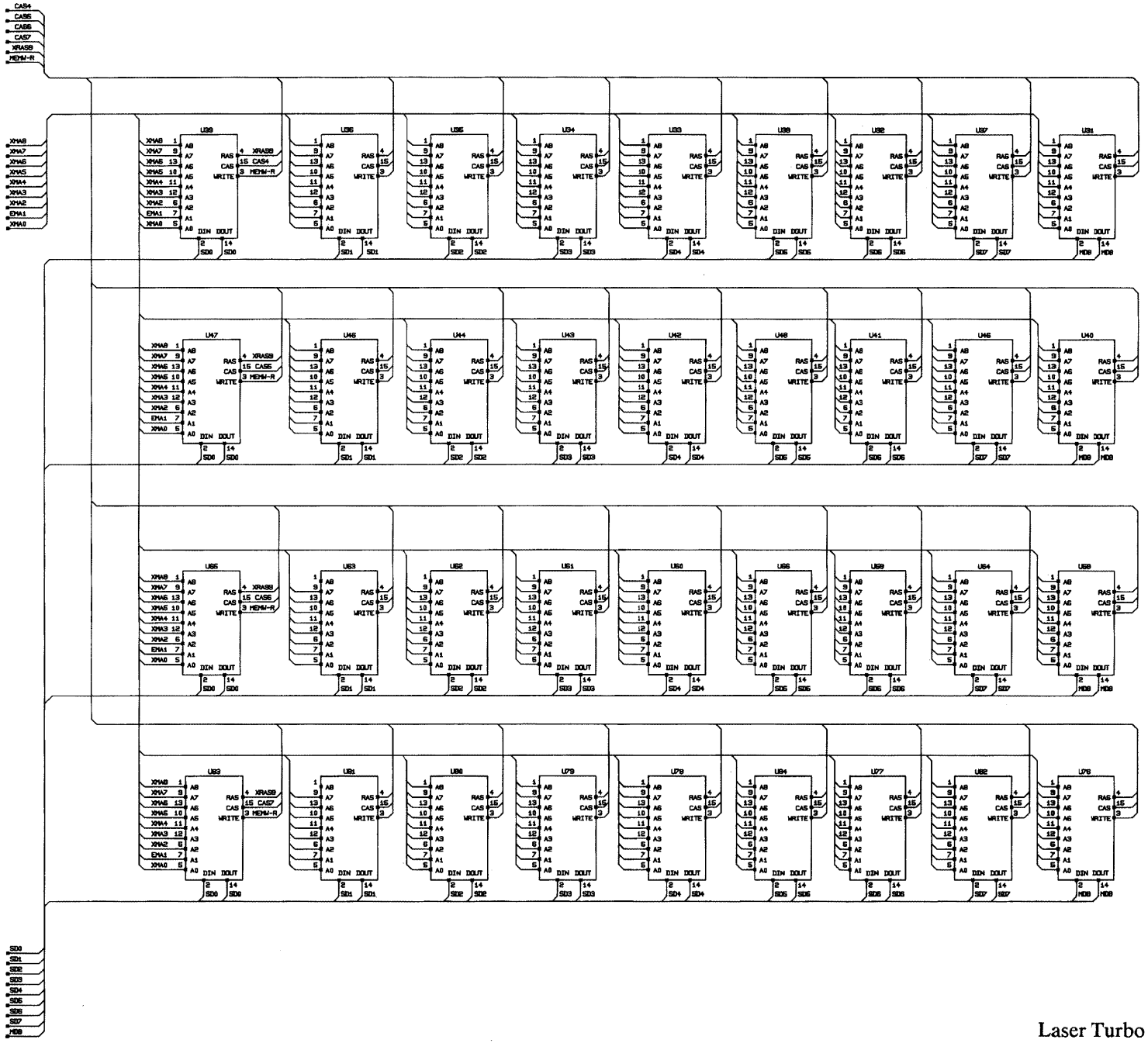
Mnemonic	Full Name
WAIT	WAIT
XCHG	Exchange
XLAT	Translate
XOR	Exclusive OR

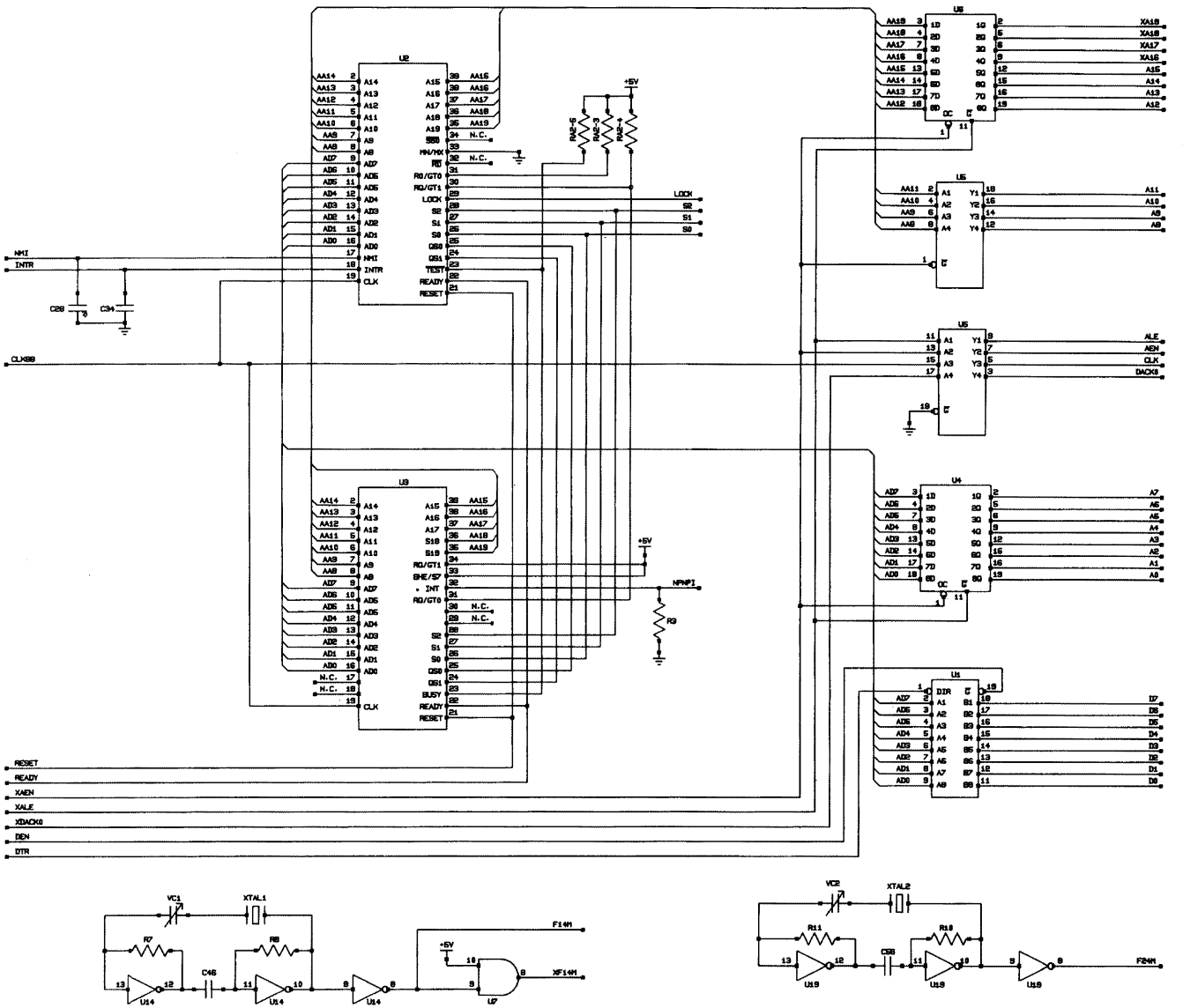
APPENDIX D

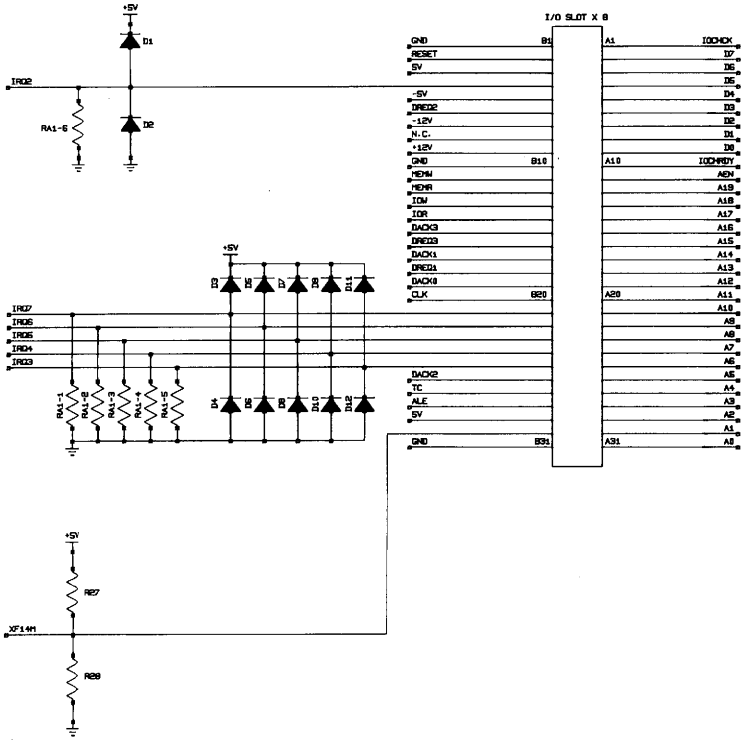
TURBO XT SCHEMATICS

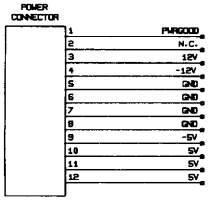


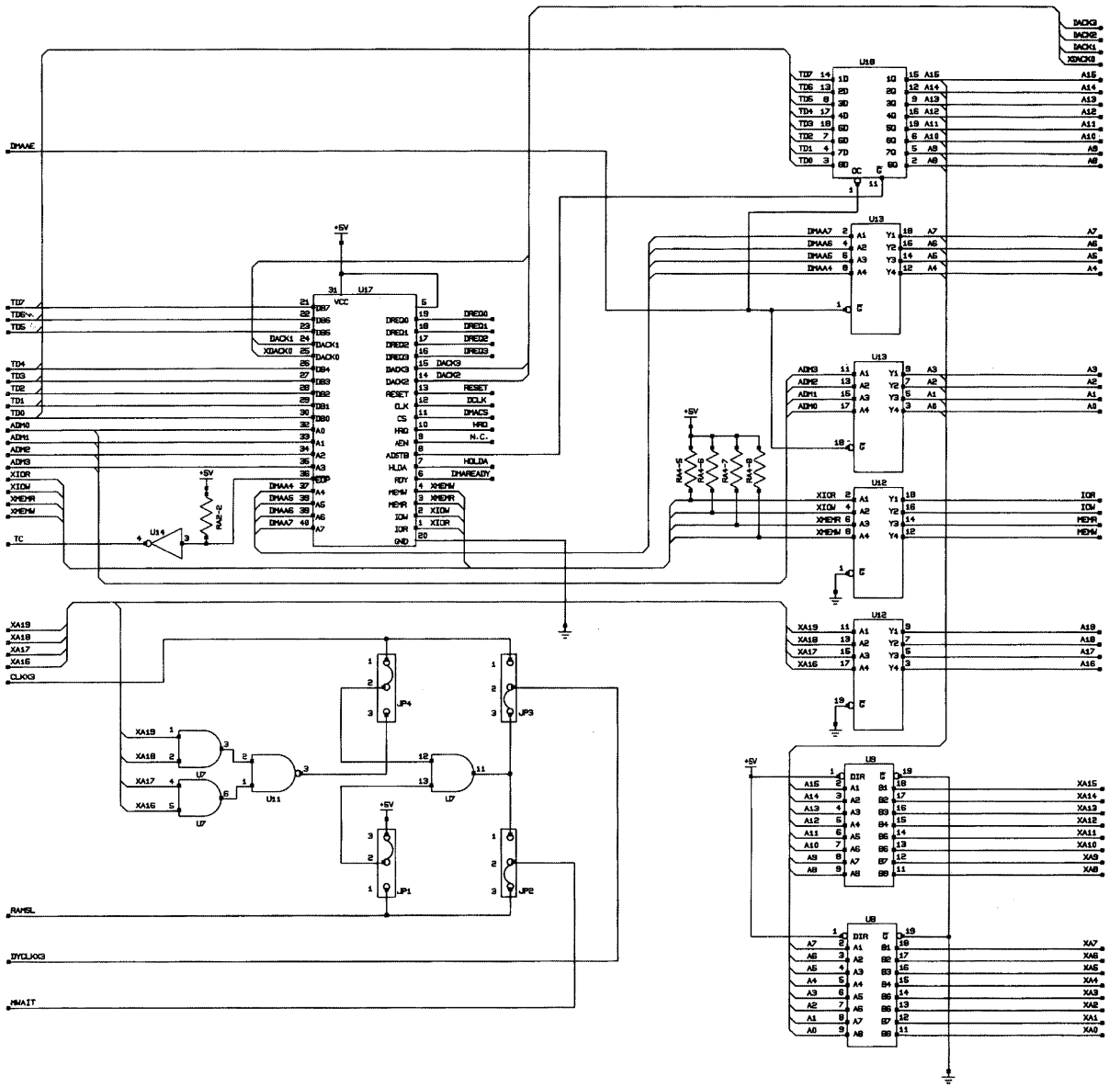


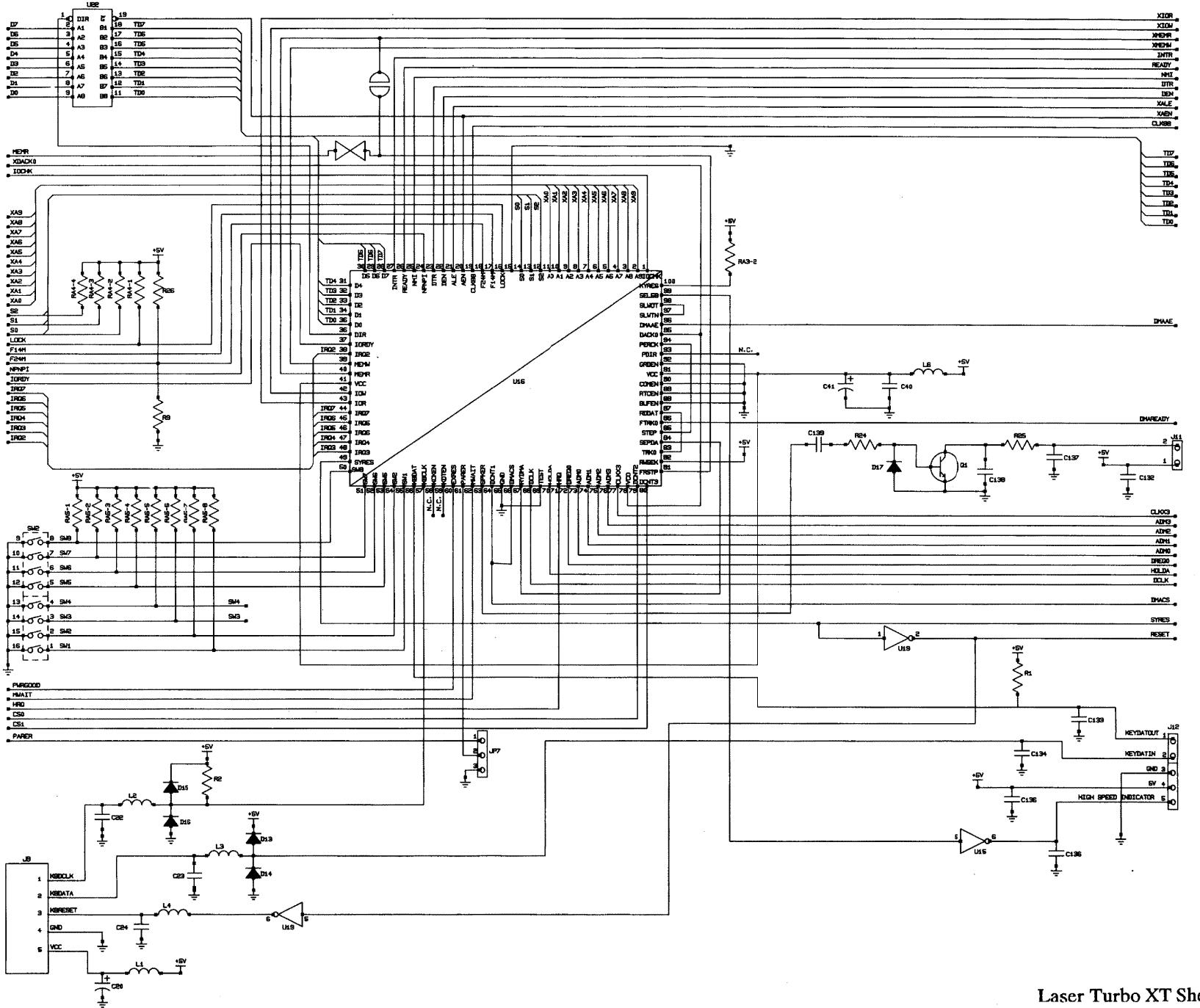



U2
U3
U8
U5
U5
U4
U1
NMI
INTR
CLK88
C28
C34
LOCK
S2
S1
S0
+5V
RN2-5
RN2-3
RN2-4
NPNPI
R9
RESET
READY
XAEN
XALE
XDACK0
DEN
DTR
XA19
XA18
XA17
XA16
A15
A14
A13
A12
A11
A10
A9
A8
ALE
AEN
CLK
DACK0
A7
A6
A5
A4
A3
A2
A1
A0
D7
D6
D5
D4
D3
D2
D1
D0
VC1
XTAL1
R7
R8
C46
U14
F14M
XF14M
U7
VC2
XTAL2
R11
R10
C88
U19
F24M


+5V
D1
D2
IRQ2
RA1-6
I/O SLOT X 8
GND
RESET
5V
-5V
DREQ2
-12V
N.C.
+12V
GND
MEMW
MEMR
IOW
IOR
DACK3
DREQ3
DACK1
DREQ1
DACK0
CLK
DACK2
TC
ALE
5V
GND
IOCHCK
IOCHRDY
AEN
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
RA1-7
RA1-8
RA1-3
RA1-4
RA1-5
D3
D5
D7
D9
D11
D4
D6
D8
D10
D12
R27
R28
XF14M


POWER CONNECTOR
PWRGOOD
N.C.
12V
-12V
GND
GND
GND
GND
-5V
5V
5V
5V

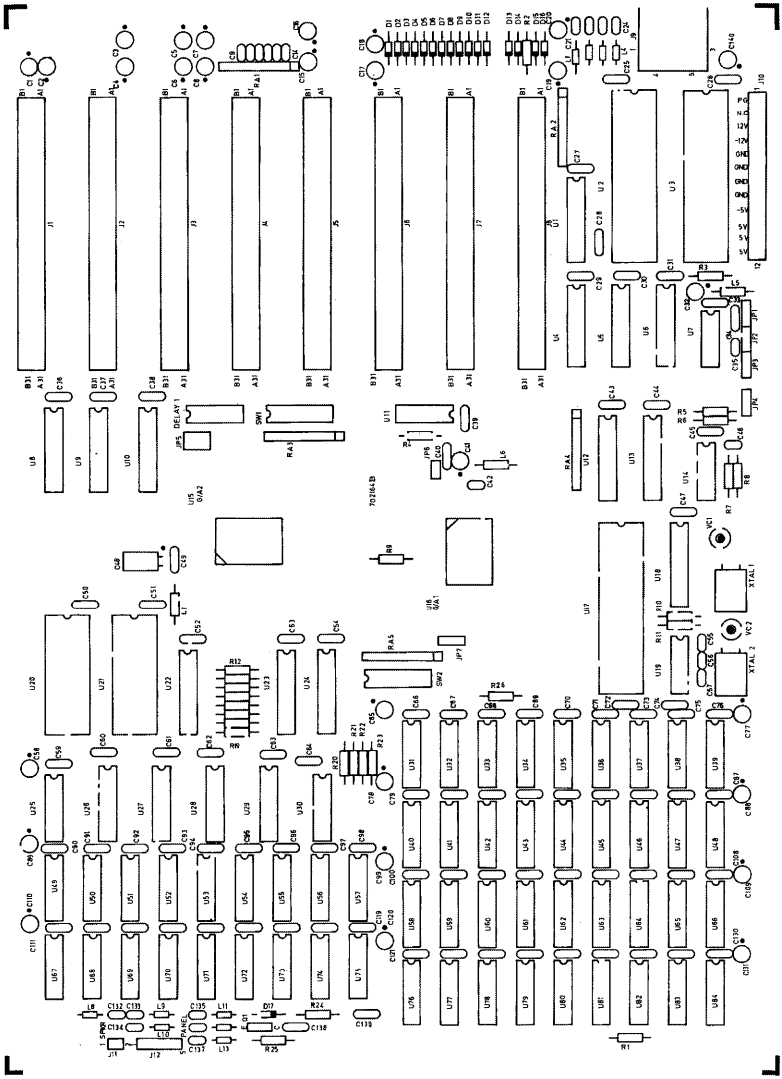




APPENDIX E

TURBO XT PART LISTS

APPENDIX E
TURBO XT PART LISTS



LASER Turbo XT Main Board Component Location List:

DISTINATION	PART NUMBER	DESCRIPTION
U1,U8-U10, U22	27-0100-00-01 V27-0100-00-04	74LS245 (MOTOROLA) 74LS245 (TEXAS)
U2	27-0554-01-01	MBL8088-1 (10MHZ) (FUJITSU)
	V27-0554-01-00	P8088-1 (10MHZ) (AMD)
AND	40-0008-00-03	40 PINS I.C. SOCKET (DOUBLE CONTACT)
	40-0008-00-00	40 PINS I.C. SOCKET (DOUBLE CONTACT)
U3	40-0008-00-03	40 PINS I.C. SOCKET (DOUBLE CONTACT)
	V40-0008-00-00	40 PINS I.C. SOCKET (DOUBLE CONTACT)
U4,U6,U18	27-0183-00-00	74LS373 (HITACHI)
	V27-0183-00-01	74LS373 (MOTOROLA)
	V27-0183-00-02	74LS373N (TEXAS)
U5,U12,U13	27-0160-00-00	74LS244 (MOTOROLA)
U7	27-0184-00-00	74LS08 (HITACHI)
	V27-0184-00-04	74LS08 (TEXAS)
	V27-0184-00-05	74LS08 (MOTOROLA)
U11	27-0037-01-00	HD74LS00N (NITACHI)
	V27-0037-01-03	74LS00 (MOTOROLA)
	V27-0037-01-06	74LS00 (MOTOROLA)
	V27-0037-01-07	74LS00N (TEXAS)
U14	27-0038-02-00	HD74LS04 (HITACH)
	V27-0038-02-03	74LS04 (MOTOROLA)
	V27-0038-02-05	74LS04N
	V27-0038-02-06	74LS04 (SGS)
U15	27-0603-00-00	GATE ARRAY A2
U16	27-0602-01-00	GATE ARRAY A1.1
	R27-0602-00-00	GATE ARRAY A1
U17	27-0488-00-00	8237A-5 DMA CONTROLLER (NEC)
	V27-0488-00-01	P8237A-5 DMA CONTROLLER (AMD)
	V27-0488-00-02	P8237A-5 DMA CONTROLLER (INTEL)

DISTINATION	PART NUMBER	DESCRIPTION (continued)
U19	27-0038-03-00	74S04 (TEXAS)
	V27-0038-03-03	HD74S04 (HITACHI)
U20	27-0672-00-03	MASK ROM R09864D-196 (200NS)
	A27-0143-03-00	EPROM 2764-20 (200NS) (HITACHI)
	A27-0143-02-04	EPROM TMS2764-25 (250NS)(TEXAS)
AND	40-0007-00-04	28 PINS I.C. SOCKET (DOUBLE CONTACT)
	V40-0007-00-00	28 PINS I.C. SOCKET (DOUBLE CONTACT)
	V40-0007-00-02	28 PINS I.C. SOCKET (DOUBLE CONTACT)
U21	40-0007-00-04	28 PINS I.C. SOCKET (DOUBLE CONTACT)
	V40-0007-00-00	28 PINS I.C. SOCKET (DOUBLE CONTACT)
	V40-0007-00-02	28 PINS I.C. SOCKET (DOUBLE CONTACT)
U23,U24	27-0451-00-00	74S244 (TEXAS)
U26-U29	40-0067-00-03	18 PINS I.C. SOCKET (DOUBLE CONTACT)
	A40-0067-01-00	18 PINS I.C. SOCKET (DOUBLE CONTACT)
U25,U30, U31-U39	40-0082-01-01	16 PINS I.C. SOCKET (DOUBLE CONTACT)
U40-U48, U49-U57,	A40-0625-16-00	16 PINS I.C. SOCKET (DOUBLE CONTACT)
U58-U66, U76-U84	V40-0082-01-00	16 PINS I.C. SOCKET (DOUBLE CONTACT)
U67-U75	27-0532-03-00	DRAM HM50256P-12 (256K X 1) (HITACHI)
	V27-0532-03-01	DRAM MT1259-12 (256K X 1) (MICRON)
	V27-0532-03-02	DRAM MCM6256AP12 (256K X 1)(MOTOROLA)
	V27-0532-03-03	DRAM TMM41256P-12 (256K X 1)(TOSHIBA)
	V27-0632-03-04	DRAM KM41256-12 (256K X 1)(SAMSUNG)
AND	40-0082-01-01	16 PINS I.C. SOCKET (DOUBLE CONTACT)
	V40-0082-01-00	16 PINS I.C. SOCKET (DOUBLE CONTACT)
	A40-0082-01-00	16 PINS I.C. SOCKET (DOUBLE CONTACT)
R1,R2	23-0472-10-02	RESISTOR 4.7K OHM 1/4W +/-5%
	V23-0472-10-00	RESISTOR 4.7K OHM 1/4W +/-5%

DISTINATION	PART NUMBER	DESCRIPTION (continued)
R3	23-0015-10-02	RESISTOR 100K OHM 1/4W +/-5%
	V23-0015-10-00	RESISTOR 100K OHM 1/4W +/-5%
R4,R12-R23	23-0270-10-02	RESISTOR 27K OHM 1/4W +/-5%
R5,R6	(NOT USD)	
R7,R8	23-0013-10-02	RESISTOR 1K OHM 1/4W +/-5%
	V23-0013-10-00	RESISTOR 1K OHM 1/4W +/-5%
R9,R26	23-0561-10-02	RESISTOR 560 OHM 1/4W +/-5%
R10,R11	23-0221-10-02	RESISTOR 220 OHM 1/4W +/-5%
	V23-0221-10-00	RESISTOR 220 OHM 1/4W +/-5%
R24	23-0222-10-02	RESISTOR 2.2K OHM 1/4W +/-5%
	V23-0222-10-00	RESISTOR 2.2K OHM 1/4W +/-5%
R25	23-0470-10-02	RESISTOR 47 OHM 1/4W +/-5%
RA1	26-1103-08-01	RESISTOR NETWORK 10K OHM X 8,9 PINS
	V26-1103-08-05	RESISTOR NETWORK 10K OHM X 8,9 PINS
RA2,RA3,RA5	26-1472-08-13	RESISTOR NETWORK 4.7K OHM X 8,9 PINS
	V26-1472-08-00	RESISTOR NETWORK 4.7K OHM X 8,9 PINS
	V26-1472-08-01	RESISTOR NETWORK 4.7K OHM X 8,9 PINS
	V26-1472-08-02	RESISTOR NETWORK 4.7K OHM X 8,9 PINS
	V26-1472-08-05	RESISTOR NETWORK 4.7K OHM X 8,9 PINS
RA4	26-1332-08-06	RESISTOR NETWORK 3.3K OHM X 8,9 PINS
	V26-1332-08-00	RESISTOR NETWORK 3.3K OHM X 8,9 PINS
XTAL 1	25-3015-00-00	CRYSTAL 14.31818 MHZ +/-30PPM
	V25-3015-00-04	CRYSTAL 14.31818 MHZ +/-30PPM
XTAL 2	25-3063-00-01	CRYSTAL 30 MHZ +/-30PPM
	V25-3063-00-00	CRYSTAL 30 MHZ +/-30PPM
Q1	20-0028-02-00	TRANSISTOR NA31XJ
	A20-0028-04-00	TRANSISTOR NA31XI/J/H

DISTINATION	PART NUMBER	DESCRIPTION (continued)
L2-L4	25-1109-00-00	3 1/2T FERRITE BEAD CHOKE HOR.
	V25-1109-00-01	3 1/2T FERRITE BEAD CHOKE HOR.
L1,L5-L7	25-1020-00-00	CHOKE COIL 3.3UH
	V25-1020-00-02	CHOKE COIL 3.3UH
L8-L13	(SHORTED IN PCB)	
D1-D17	21-0001-00-00	DIODE IN4148
SW1,SW2	42-0055-00-00	DIP SWITCH 8 POLES (SLIDE TYPE)
	V42-0055-00-04	DIOP SWITCH 8 POLES (SLIDE TYPE)
	V42-0055-00-06	DIP SWITCH 8 POLES (SLIDE TYPE)
VC1,VC2	22-7002-01-00	TRIMMER CAP 4PF-20PF +80-0%
	A22-7002-00-00	TRIMMER CAP 20FP
	V22-7002-00-12	TRIMMER CAP 20PF
C2-C5,	22-1470-21-03	ELEC CAP 47UF 16V +/-20%
C65,C99,	V22-1470-21-11	ELEC CAP 47UF 16V +/-20%
C120	V22-1470-21-16	ELEC CAP 47UF 16V +/-20%
C19-C20	22-1100-21-00	ELEC CAP 10UF 16V +/-20%
C21-C24	22-3102-28-00	CER CAP 0.001UF 50V +80/-20%
	A22-3102-26-00	CER CAP 1000PF 50V +/-10%
	A22-3102-28-15	CER CAP 1000PF 50V +80/-20%
C25-C27,C33	23-3104-28-33	MONO CAP 0.1UF 50V +80/-20%
C29-C31,	V22-3104-28-40	MONO CAP 0.1UF 50V +80/-20%
C36-C40,	V22-3104-28-53	MONO CAP 0.1UF 50V +80/-20%
C43-C45,C47, C49-C54, C59-C64, C66-C76, C79-C87, C90-C98, C100-C108, C111-C119,C121, C123-C130, C138-C139,		
C122	(NOT IN USE)	
C28	22-3471-26-00	CER CAP 470PF 50V +/-10%

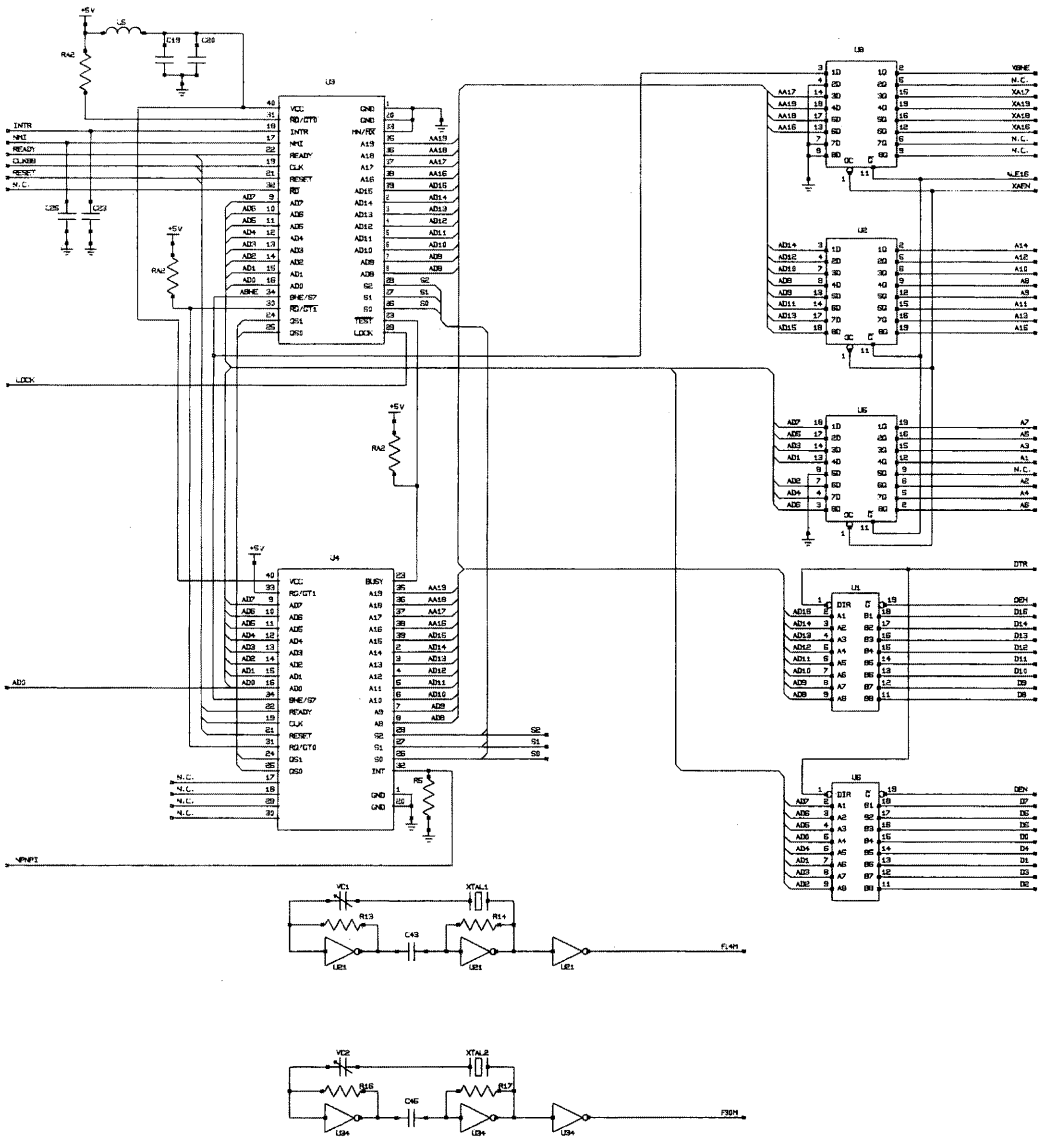
DISTINATION	PART NUMBER	DESCRIPTION (continued)
C32,C41,C48	22-1109-61-03	ELEC CAP 1UF 50V +/-20%
	V22-1109-61-04	ELEC CAP 1UF 50V +/-20%
C34	22-3331-26-00	CER CAP 330PF 50V +/-10%
C46	22-3470-26-00	CER CAP 47PF 50V +/-10%
	A22-3470-25-00	CER CAP 47PF 50V +/-5%
	A22-3470-26-01	CER CAP 47PF 50V +/-10%
C56	22-3101-26-00	CER CAP 47PF 50V +/-10%
C58,C77,C88 C89,C109, C110,C131,	22-1101-11-03	ELEC CAP 100UF 10V +/-10%
C1,C6-C8, C9-C14, C15-C18,C35, C42,C55,C57, C78,C132-C137,	(NOT USED)	
J1-J8	40-0472-00-00	PCB EDGE CONNECTOR 62 WAYS
J9	40-0459-05-00	DIN SOCKET (WITH SHIELDS) 5 PINS
J10	40-0500-12-00	HEADER (POWER)
J11	40-0118-00-01	CONNECTOR WAFER 2 JPINS (RIGHT ANGLE)
	V40-0118-00-00	CONNECTOR WAFER 2 PINS (RIGHT ANGLE)
J12	40-0120-00-01	CONNECTOR WAFER 5 PINS (RIGHT ANGLE)
	V40-0120-00-00	CONNECTOR WAFER 5 PINS (DRIGHT ANGLE)
JP1-JP5	(SHORTED IN PCB)	
JP6	(NOT USED)	
JP7	40-0215-00-01	WAFER 3 PINS
	V40-0215-00-00	WAFER 3 PINS
AND	40-0342-00-00	2-CONTACT SHORT CIRCUIT SOCKET
	A40-0342-01-00	SHUNT CONNECTOR
	A40-0342-02-00	SHUNT CONNECTOR

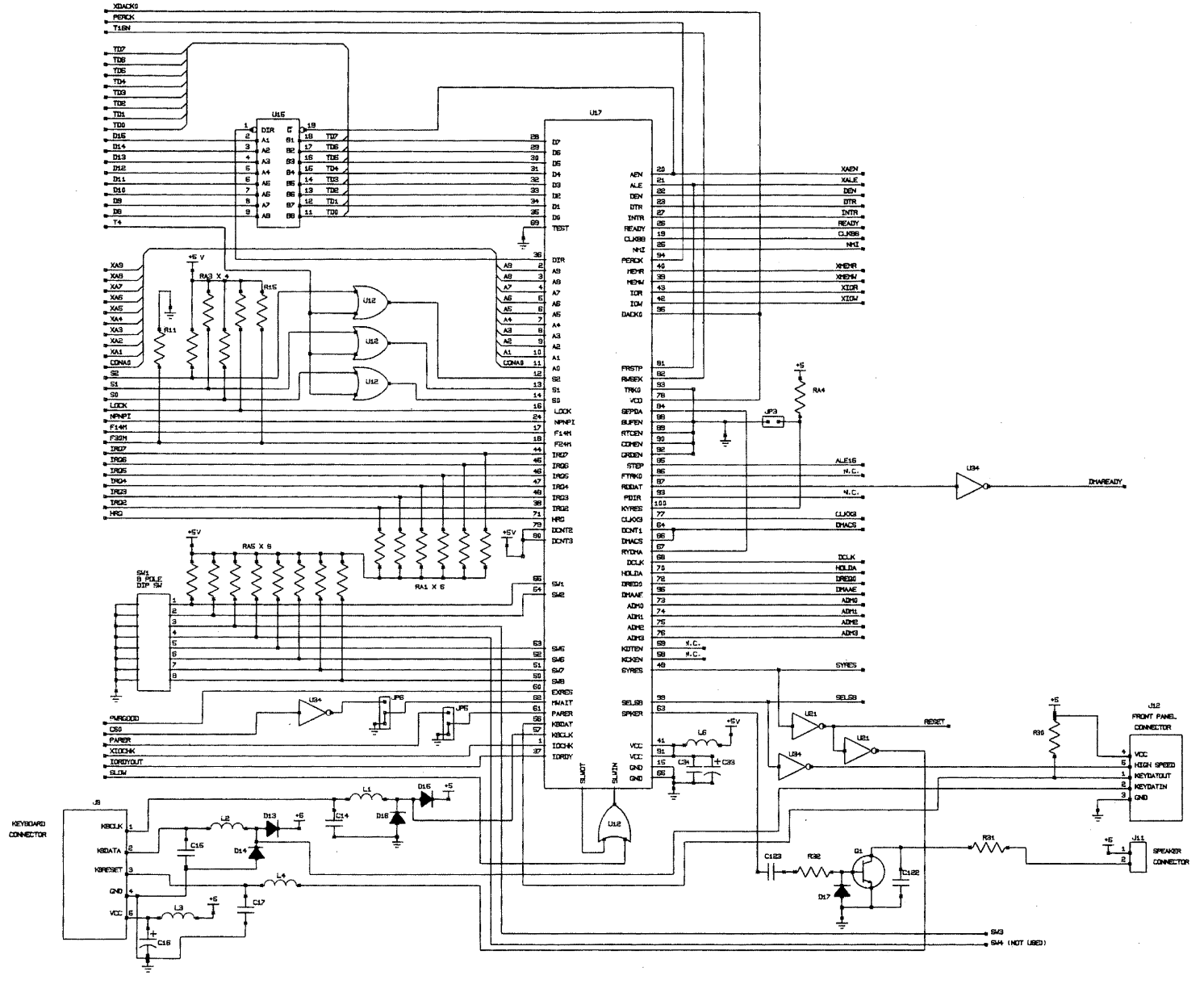
Note: *'A' placed before a part number indicates an alternative source.*

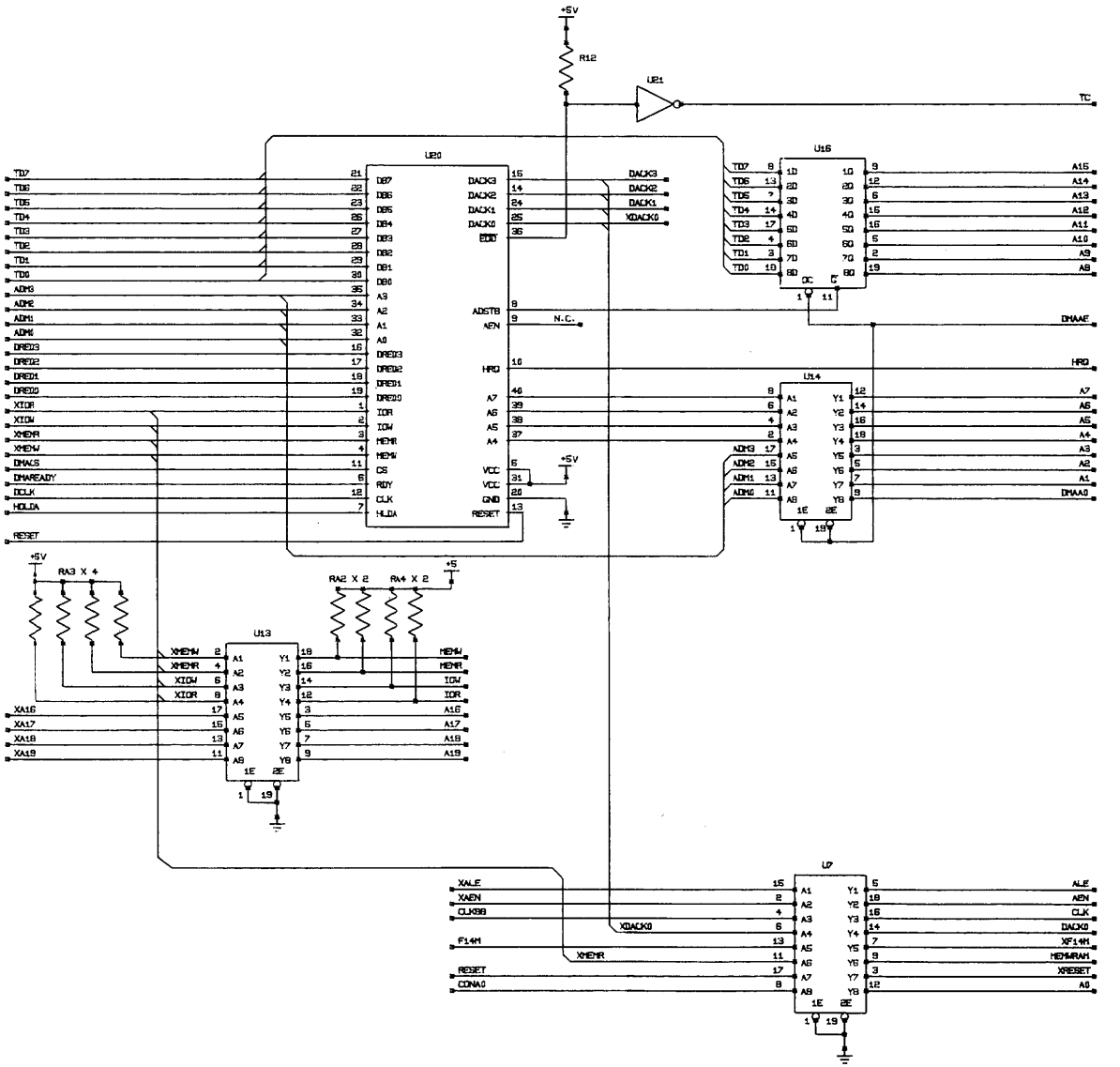
'V' placed before a part number indicates an alternative vendor.

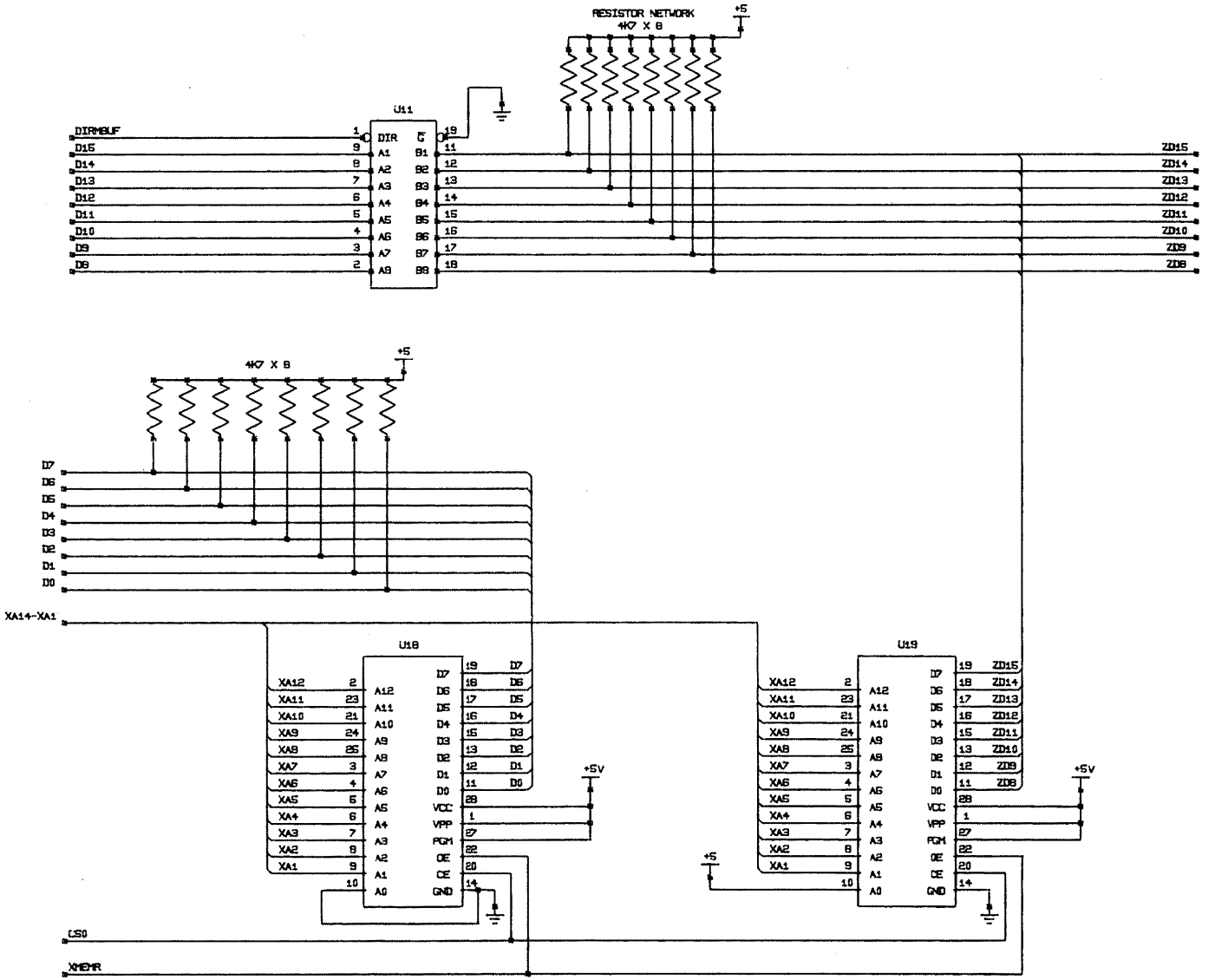
APPENDIX F

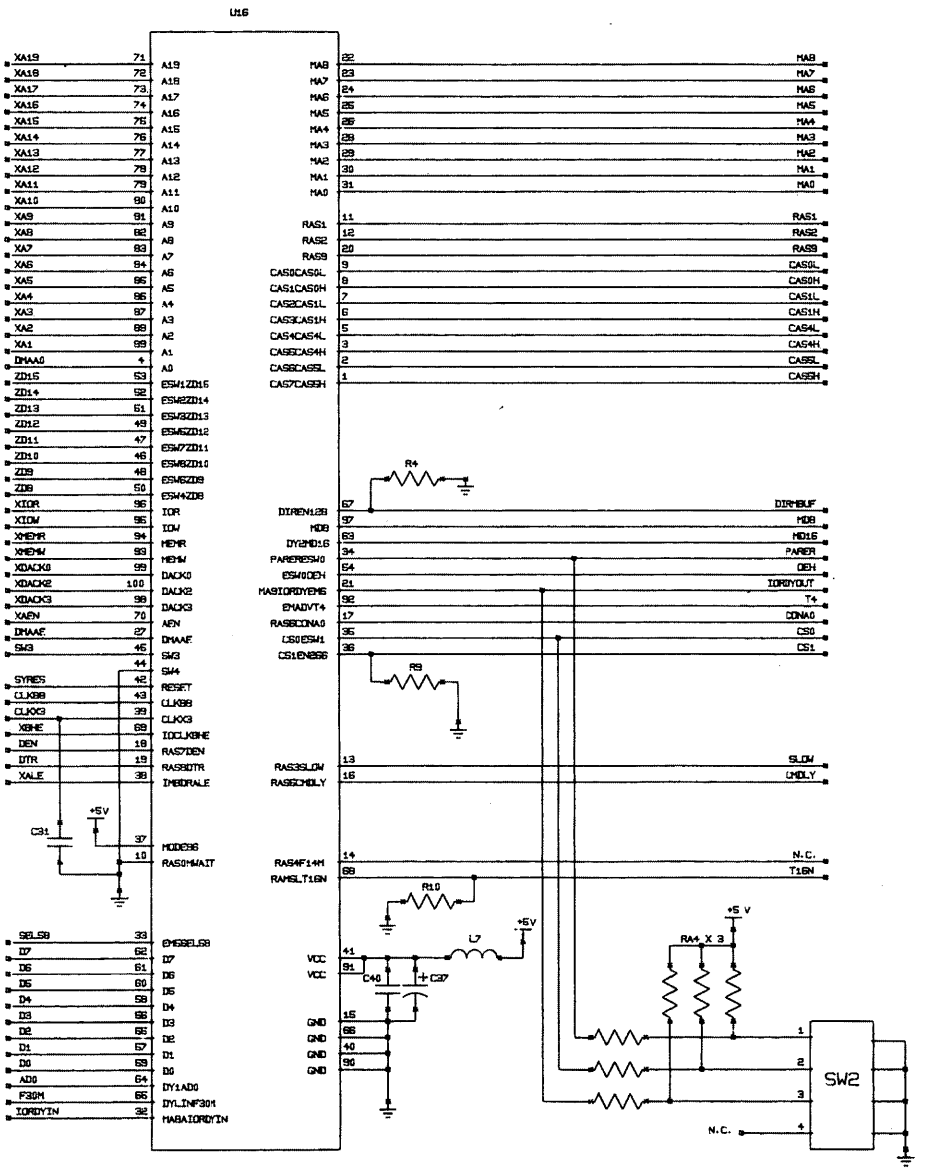
SCHEMATIC FOR TURBO XT/2 OR TURBO XT/3

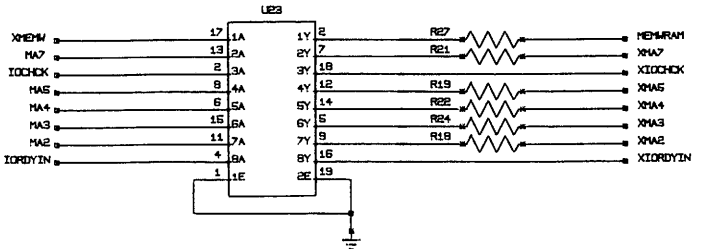


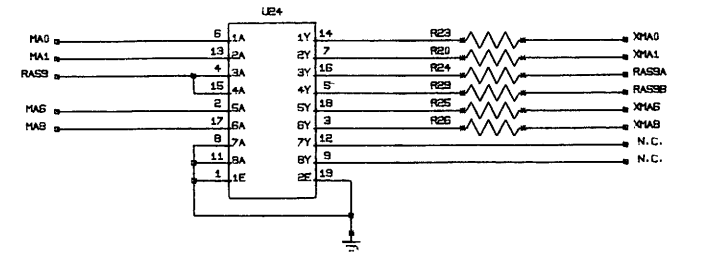

XDACK0
PERCK
T1EN
TD7
TD6
TD5
TD4
TD3
TD2
TD1
TD0
D15
D14
D13
D12
D11
D10
D9
D8
T4
U15
DIR
A1
A2
A3
A4
A5
A6
A7
A8
U17
XA9
XA8
XA7
XA6
XA5
XA4
XA3
XA2
XA1
CONA0
+5 V
RA3 X 4
R11
R15
U12
S2
S1
S0
LOCK
NPNPI
F14M
F28M
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
IRQ2
NRQ
RA5 X 6
RA1 X 6
DCNT2
DCNT3
SW1
8 POLE
DIP SW
SW2
SW5
SW6
SW7
SW8
EXRES
MWAIT
PARER
KBDAT
KBCLK
IOCHK
IORDY
PURGOOD
CS0
PARER
XIOCHK
IORDYOUT
SLOW
U34
JP6
JP5
SLWAT
SLWIN
AEN
ALE
DEN
DTR
INTR
READY
CLK88
NMI
PERCK
MEMR
MEMW
IOR
IOW
DACK0
FRSTP
RWSEK
TRK0
VCO
SEPDA
SUPEN
RTCEN
COMEN
GRDEN
STEP
FTRK0
RDDAT
PDIR
KYRES
CLKX3
DCNT1
DMACS
RYDMA
DCLK
HOLDA
DREQ0
DMAAE
ADH0
ADH1
ADH2
ADH3
KDTEN
KCKEN
SYRES
SELS8
SPKER
VCC
GND
L6
C34
C33
XAEN
XALE
DEN
DTR
INTR
READY
CLK88
NMI
XMEMR
XMEMW
XIOR
XIOW
RA4
JP3
ALE16
N.C.
CLKX3
DMACS
DCLK
HOLDA
DREQ0
DMAAE
ADH0
ADH1
ADH2
ADH3
SYRES
SELS8
U34
DMAREADY
U21
RESET
U34
R36
J12
FRONT PANEL
CONNECTOR
VCC
HIGH SPEED
KEYDATOUT
KEYDATIN
GND
J8
KEYBOARD
CONNECTOR
KBCLK
KBDATA
KBRESET
GND
VCC
L1
L2
L3
L4
D13
D14
D15
D16
C14
C15
C16
C17
+5
U12
C123
R32
Q1
C122
D17
R31
J11
SPEAKER
CONNECTOR
SW3
SW4 (NOT USED)

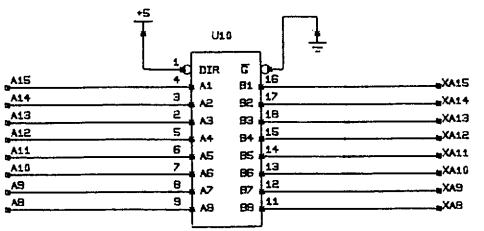

+5V
R12
U21
TC
U20
U16
U14
U13
U7
RA3 X 4
RA2 X 2
RA4 X 2
DACK3
DACK2
DACK1
XDACK0
N.C.
DMAAE
HRQ
DMAA0
RESET
XMEMW
XMEMR
XIOW
XIOR
XA16
XA17
XA18
XA19
MEMW
MEMR
IOR
A16
A17
A18
A19
XALE
XAEN
CLK99
F14M
CONA0
ALE
AEN
CLK
DACK0
XF14M
MEMWRAM
XRESET

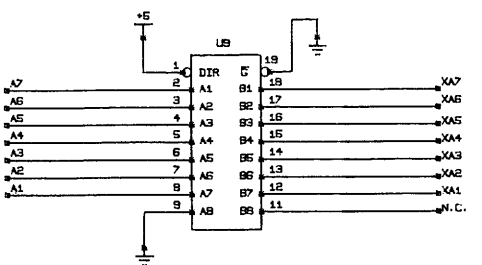

RESISTOR NETWORK
4K7 X 8
+5
U11
DIR
G
DIRBUF
D15
D14
D13
D12
D11
D10
D9
D8
A1
A2
A3
A4
A5
A6
A7
A8
B1
B2
B3
B4
B5
B6
B7
B8
ZD15
ZD14
ZD13
ZD12
ZD11
ZD10
ZD9
ZD8
4K7 X 8
+5
D7
D6
D5
D4
D3
D2
D1
D0
XA14-XA1
U18
U19
XA12
XA11
XA10
XA9
XA8
XA7
XA6
XA5
XA4
XA3
XA2
XA1
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
D7
D6
D5
D4
D3
D2
D1
D0
VCC
VPP
PGM
OE
CE
GND
+5V
+5
CS0
XMEMR

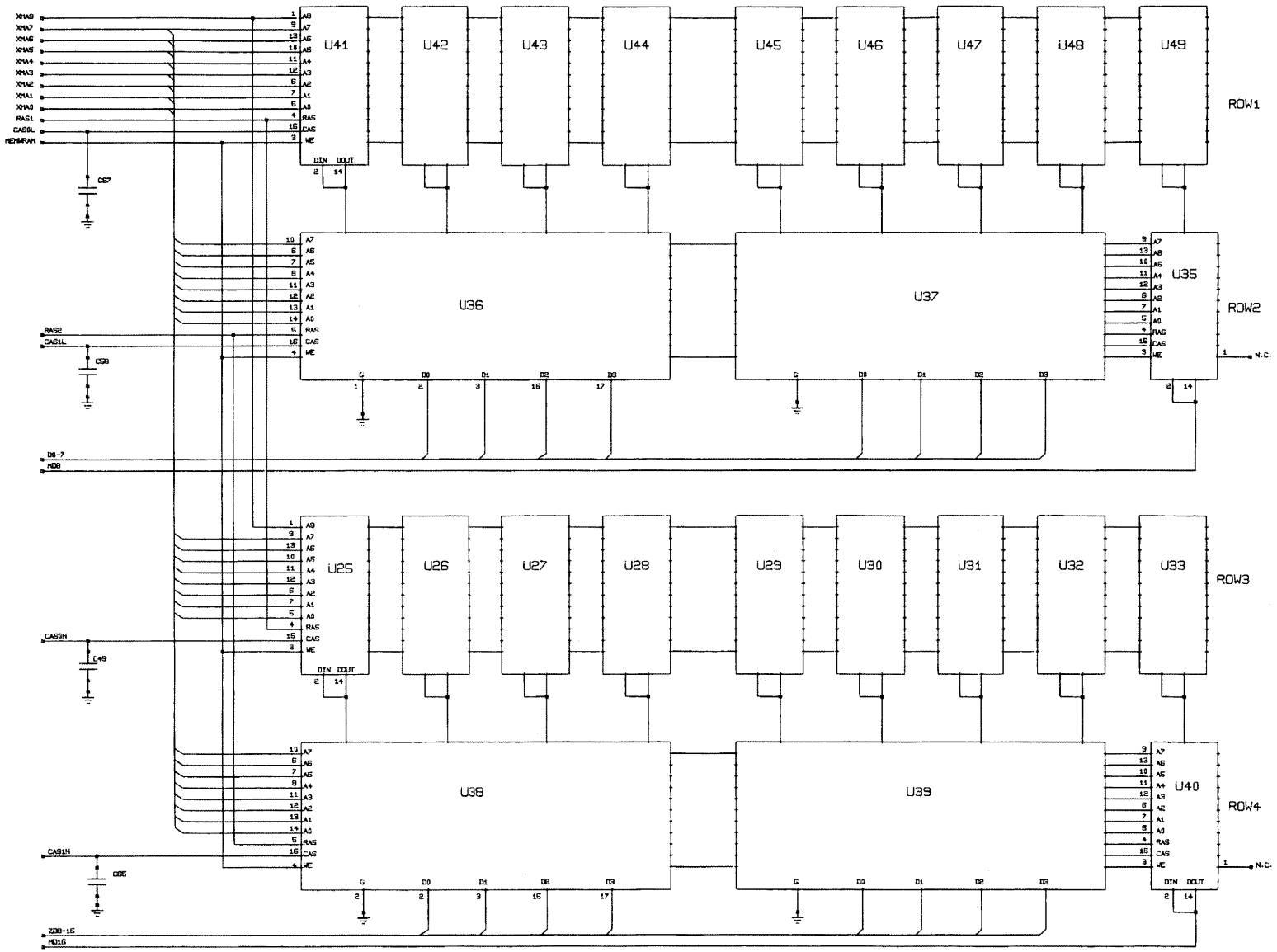

U16
XA19 71
XA18 72
XA17 73
XA16 74
XA15 75
XA14 76
XA13 77
XA12 78
XA11 79
XA10 80
XA9 81
XA8 82
XA7 83
XA6 84
XA5 85
XA4 86
XA3 87
XA2 88
XA1 89
DMAA0 4
ZD15 53
ZD14 52
ZD13 51
ZD12 49
ZD11 47
ZD10 46
ZD9 48
ZD8 50
XIOR 96
XIOW 95
XMEMR 94
XMEMW 93
XDACK0 99
XDACK2 100
XDACK3 98
XAEN 70
DMAAE 27
SW3 45
SW4 44
SYRES 42
CLK88 43
CLK33 39
XBHE 69
DEN 18
DTR 19
XALE 38
C31
+5V
37
10
SBLS8 33
D7 62
D6 61
D5 60
D4 58
D3 56
D2 55
D1 57
D0 59
AD0 64
F30M 65
IORDYIN 32
A19
A18
A17
A16
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
ESW1ZD15
ESW2ZD14
ESW3ZD13
ESW5ZD12
ESW7ZD11
ESW8ZD10
ESW6ZD9
ESW4ZD8
IOR
IOW
MEMR
MEMW
DACK0
DACK2
DACK3
AEN
DMAAE
SW3
SW4
RESET
CLK88
CLK33
IOCLKBHE
RAS7DEN
RAS8DTR
IMBDRALE
MODE36
RAS0MWAIT
EMSBELS8
D7
D6
D5
D4
D3
D2
D1
D0
DY1AD0
DYL_INF30M
MABAIORDYIN
MA8 22
MA7 23
MA6 24
MA5 25
MA4 26
MA3 28
MA2 29
MA1 30
MA0 31
RAS1 11
RAS2 12
RAS9 20
CAS0CAS0L 9
CAS1CAS0H 8
CAS2CAS1L 7
CAS3CAS1H 6
CAS4CAS4L 5
CAS5CAS4H 3
CAS6CASSL 2
CAS7CASSH 1
DIREN128 57
MD8 58
DY2MD16 63
PARERESW0 34
ESW0DEN 54
MASIORDYEMS 21
EMADVT+ 92
RASBCONA0 17
CS0ESW1 35
CS1EN8SB 36
RAS3SLOW 13
RAS8CMDLY 15
RAS4F14M 14
RAMSLT16N 88
VCC 41
VCC 91
GND 15
GND 66
GND 40
GND 90
R4
R9
R10
L7
C40
C37
+5V
+5 V
RA4 X 3
SW2
N.C.
DIRMBUF
MD8
MD16
PARER
DEN
IORDYOUT
T4
DONA0
CS0
CS1
SLOW
CMDLY
N.C.
T16N

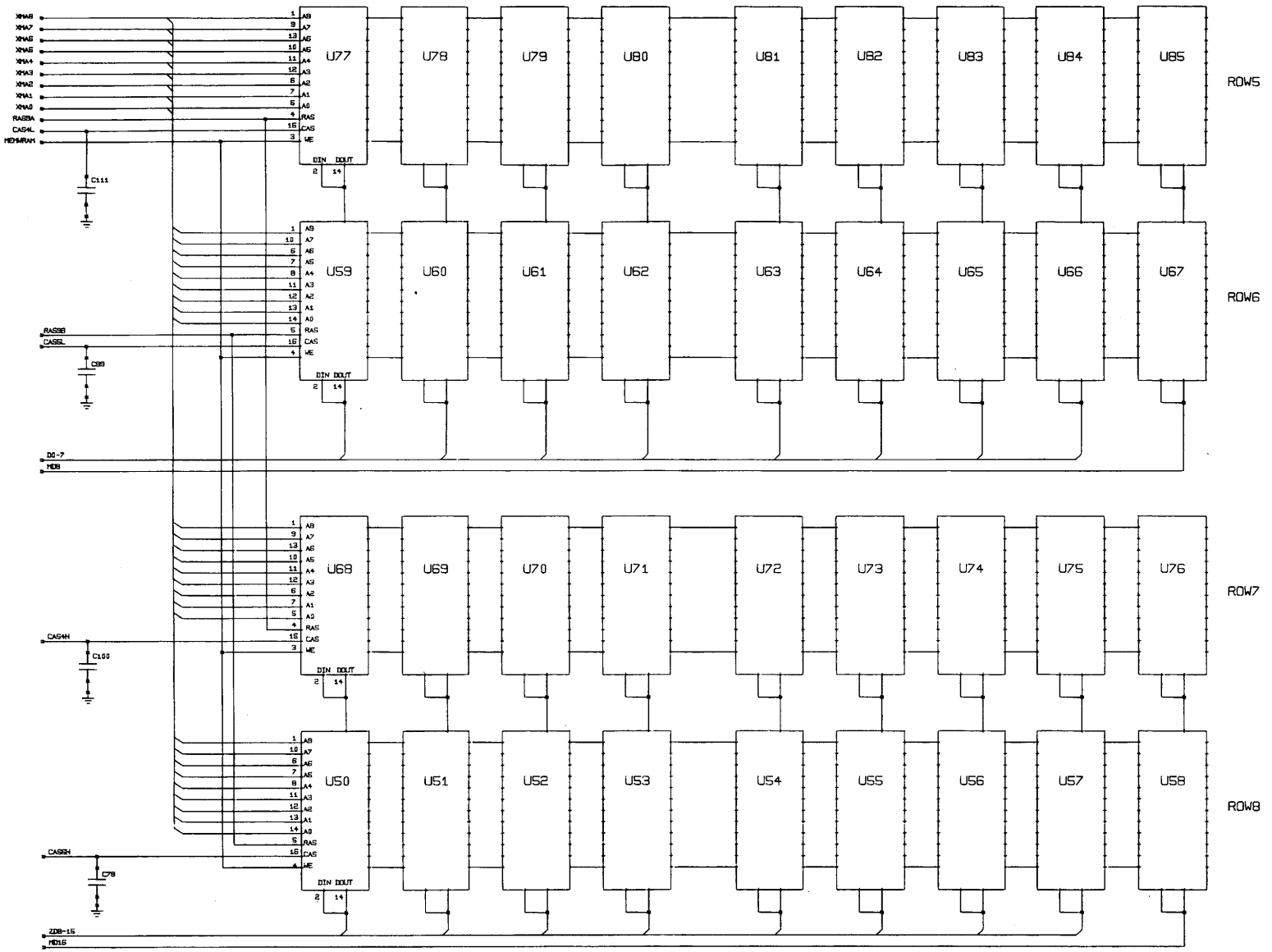

U23
XMEMW
MA7
IOCHCK
MA5
MA4
MA3
MA2
IORDYIN
R27
R21
R19
R22
R24
R18
MEM&RAM
XMA7
XIOCHCK
XMA5
XMA4
XMA3
XMA2
XIORDYIN

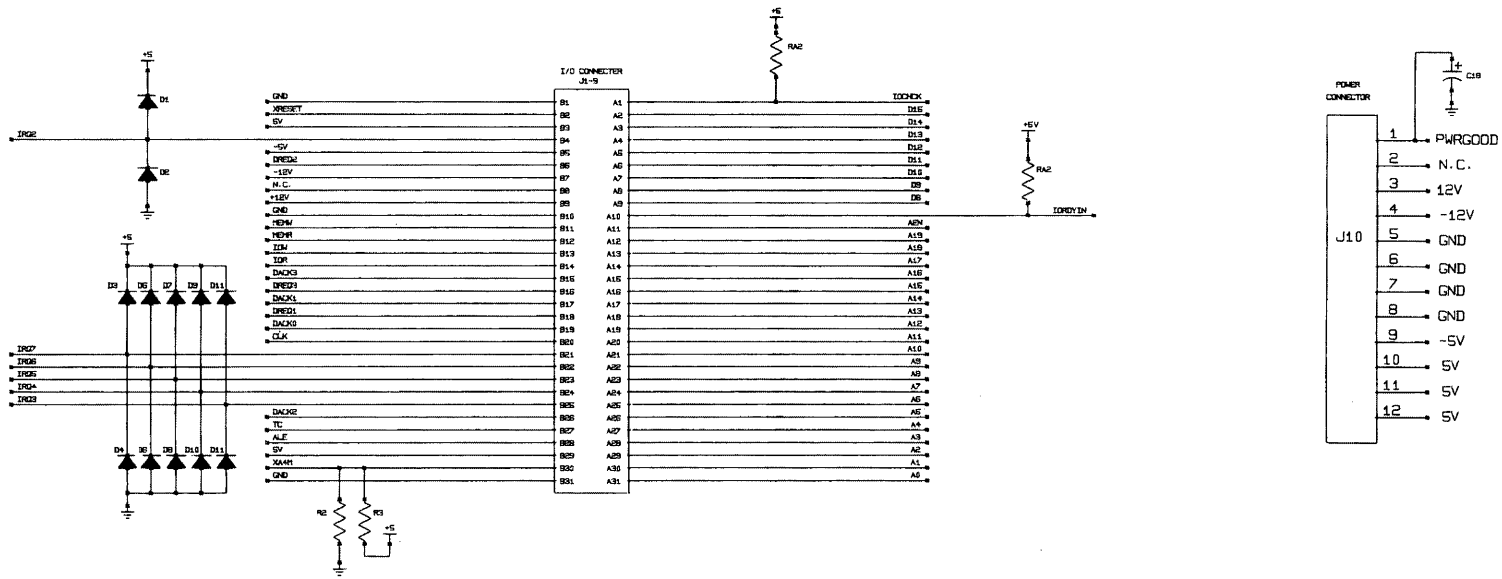

U24
MA0
MA1
RAS9
MA6
MA8
R23
R20
R24
R29
R25
R26
XMA0
XMA1
RAS9A
RAS9B
XMA6
XMA8
N.C.
N.C.


+5
U10
DIR
A15
A14
A13
A12
A11
A10
A9
A8
XA15
XA14
XA13
XA12
XA11
XA10
XA9
XA8


+5
U9
DIR
A7
A6
A5
A4
A3
A2
A1
XA7
XA6
XA5
XA4
XA3
XA2
XA1
N.C.


U41
U42
U43
U44
U45
U46
U47
U48
U49
ROW1
U36
U37
U35
ROW2
U25
U26
U27
U28
U29
U30
U31
U32
U33
ROW3
U38
U39
U40
ROW4
RAS2
CAS1L
CAS0H
CAS1H
D0-7
MD8
ZD9-15
MD16
N.C.


U77
U78
U79
U80
U81
U82
U83
U84
U85
ROW5
U59
U60
U61
U62
U63
U64
U65
U66
U67
ROW6
U68
U69
U70
U71
U72
U73
U74
U75
U76
ROW7
U50
U51
U52
U53
U54
U55
U56
U57
U58
ROW8
RASSB
CASSL
CASSH
CASSL
D0-7
MD8
ZD8-15
MD15
C111
C99
C100
C78

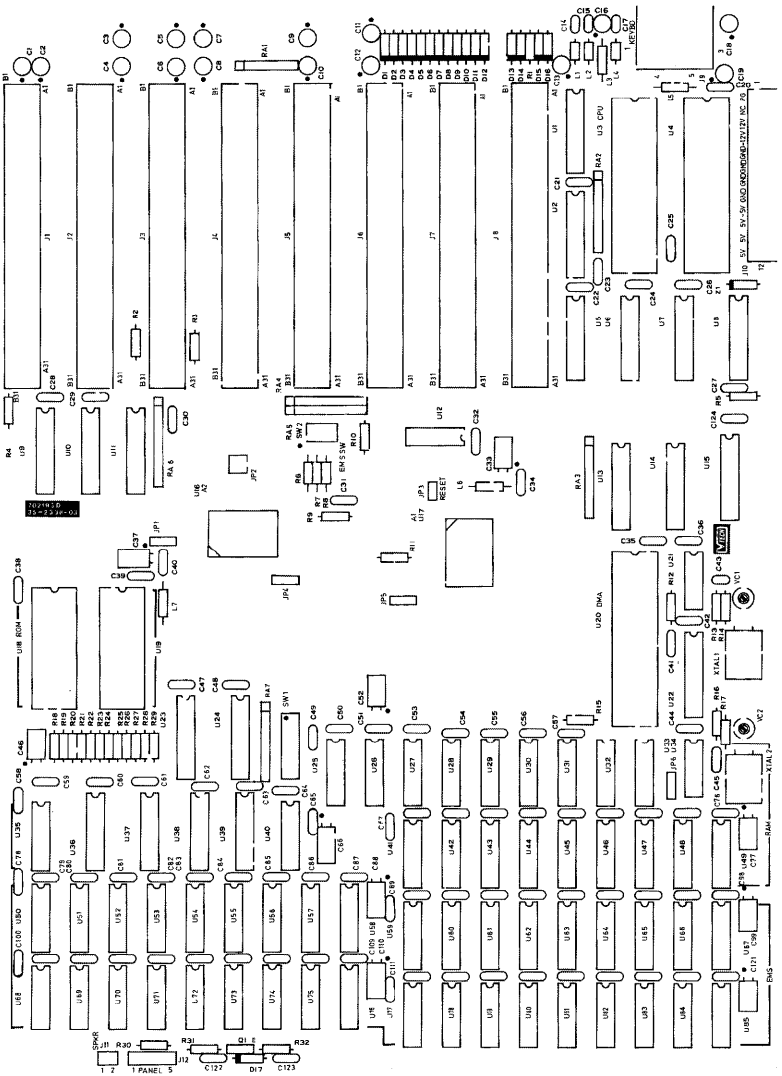

I/O CONNECTER
J1-9
RA2
RA2
+5V
IOCHCK
IORDYIN
GND
XRESET
5V
-5V
DRED2
-12V
N.C.
+12V
GND
MEMW
MEMR
IOW
IOR
DACK3
DRED3
DACK1
DRED1
DACK0
CLK
DACK2
TC
ALE
5V
XAH1
GND
IRQ2
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
D1
D2
D3
D6
D7
D9
D11
D4
D5
D8
D10
D12
R2
R3
+5

POWER
CONNECTOR
C19
J10
1 PWRGOOD
2 N.C.
3 12V
4 -12V
5 GND
6 GND
7 GND
8 GND
9 -5V
10 5V
11 5V
12 5V

APPENDIX G

PART LIST FOR TURBO XT/2
OR TURBO XT/3

APPENDIX G
TURBO XT/2 OR XT/3 PART LISTS



LASER Turbo XT/2 And XT/3 : Main Board Component Location List

DESTINATION	PART NUMBER	DESCRIPTION
U1,6,9-11,15	27-0100-00-04	74LS245 (TEXAS)
	V27-0100-00-01	74LS245 (MOTOROLA)
U2,5,8,22	27-0183-00-02	74LS373N (TEXAS)
	V27-0183-00-00	74LS373 (HITACHI)
	V27-0183-00-01	74LS373 (MOTOROLA)
U3	27-0737-00-00	MBL8006 - 1 (FUJITSU)
and SOCKET X 2	40-0008-00-03	40 PINS I.C. SOCKET
(one for 8087)	V40-0008-00-00	40 PINS I.C. SOCKET
	A40-0625-40-07	40 PINS I.C. SOCKET
	A40-0625-40-09	40 PINS I.C. SOCKET
U7,13,14,23,24	27-0160-00-03	74LS244 (TEXAS)
	V27-0160-00-00	74LS244 (MOTOROLA)
U12	27-0087-02-00	74S32 (TEXAS)
U16	27-0771-00-00	GATE ARRAY A2.1
U17	27-0602-01-00	GATE ARRAY A1.1
U18,19	27-0876-00-00	MASK ROM 2364C-200ns (GOULD)
	R27-0143-08-01	EPROM HY27C64-20 (HYUNDAI)
	R27-0143-02-04	EPROM TMS2764-25 (TEXAS)
and SOCKET X 2	40-0007-00-04	28 PINS I.C. SOCKET
	V40-0007-00-00	28 PINS I.C. SOCKET
	V40-0007-00-02	28 PINS I.C. SOCKET
	A40-0625-28-07	28 PINS I.C. SOCKET
U20	27-0488-00-03	SAB8237A - 5 (SIMENS) DMA CONTROLLER
	V27-0488-00-02	P8237A-5 (INTEL) DMA CONTROLLER
	V27-0488-00-00	8237A-5 (NEC) DMA CONTROLLER
	V27-0488-00-01	P82371-5 (AMD) DMA CONTROLLER
	A27-0488-01-00	UM8237AE-5 (UMC) DMA CONTROLLER
U21	27-0038-02-00	HD74LS04 (HITACHI)
	V27-0038-02-03	74LS04 (MOTOROLA)
	V27-0038-02-05	74LS04N (TEXAS)
	V27-0038-02-06	74LS04 (SGS)

DESTINATION	PART NUMBER	DESCRIPTION (continued)
U25-33,41-49	27-0532-03-00	DRAM HM50256P-12 (120ns) (HITACHI)
	V27-0532-03-01	MT1259-12 (120ns) (MICRON)
	V27-0532-03-02	MCM6256AP12 (120ns) (MOTOROLA))
	V27-0532-03-03	TMM41256P-12 (120ns) (TOSHIBA)
	V27-0532-03-04	KM41256AP-12 (120ns) (SAMSUNG)
	A27-0532-04-00	UPD41256C-10 (100ns) (NEC)
	A27-0532-04-01	MB81256-10 (100ns) (HITACHI)
and SOCKET X 56	40-0082-01-01	16-PINS I.C. SOCKET
(including	A40-0625-16-05	16 PINS I.C. SOCKET
EMS SOCKET)	V40-0082-01-00	16 PINS I.C. SOCKET
	A40-6025-16-00	16 PINS I.C. SOCKET
	A40-0625-16-03	16 PINS I.C. SOCKET
	A40-0625-16-09	16 PINS I.C. SOCKET
U34	27-0038-03-00	74S04 (TEXAS)
	V27-0038-03-03	HD74S04 (HITACHI)
U36-39	27-0597-01-00	DRAM HM5046P-12 (120ns) (HITACHI)
	V27-0597-01-01	TMM41464P-12 (120ns) (TOSHIBA)
	V27-0597-01-02	MT4067-12 (120ns) (MICRON)
	V27-0597-01-03	UPD41464-12 (120ns) (NEC)
	V27-0597-01-04	TMS446-12NL (120ns) (TEXAS)
and SOCKET X 4	40-0625-18-03	18 PINS I.C. SOCKET
	A40-0067-00-03	18 PINS I.C. SOCKET
	A40-0067-01-00	18 PINS I.C. SOCKET
	A40-0625-18-05	18 PINS I.C. SOCKET
	A40-0625-18-07	18 PINS I.C. SOCKET
	A40-0625-18-09	18 PINS I.C. SOCKET
RA1	26-1103-06-13	10K ohm X 6 RES NETWORK
	V26-1103-06-01	10K ohm X 6 RES NETWORK
	V26-1103-06-05	10K ohm X 6 RES NETWORK
RA2,RA5	26-1472-08-13	4K7 ohm X 8 RES NETWORK
	V26-1472-08-00	4K7 ohm X 8 RES NETWORK
	V26-1472-08-01	4K7 ohm X 8 RES NETWORK
	V26-1472-08-02	4K7 ohm X 8 RES NETWORK
	V26-1472-08-05	4K7 ohm X 8 RES NETWORK
RA3	26-1332-08-13	3K3 ohm X 8 RES NETWORK
	V26-1332-08-16	3K3 ohm X 8 RES NETWORK
	V26-1332-08-06	3K3 ohm X 8 RES NETWORK
	V26-1332-08-00	3K3 ohm X 8 RES NETWORK
RA4	26-1472-06-01	4K7 ohm X 6 RES NETWORK
R1,6,8-10,12,30	23-0472-10-02	4K7 ohm RESISTOR (TAPE)
	V23-0472-10-00	4K7 ohm RESISTOR

DESTINATION	PART NUMBER	DESCRIPTION (Continued)
R2,3	23-0013-10-02	1K ohm RESISTOR (TAPE)
	V23-0013-10-00	1K ohm RESISTOR
R4	23-0821-10-02	820 ohm RESISTOR (TAPE)
	V23-0821-10-00	820 ohm RESISTOR
R5	23-0015-10-02	100K ohm RESISTOR (TAPE)
	V23-0015-10-00	100K ohm RESISTOR
R7	23-0122-10-02	1.2K ohm RESISTOR (TAPE)
	V23-0122-10-00	1.2K ohm RESISTOR
R11,15	23-0561-10-02	560 ohm RESISTOR (TAPE)
	V23-0561-10-00	560 ohm RESISTOR
R13,14	23-0013-10-02	1K ohm RESISTOR (TAPE)
	V23-0013-10-00	1K ohm RESISTOR
R16,17	23-0221-10-02	220 ohm RESISTOR (TAPE)
	V23-0221-10-00	220 ohm RESISTOR
R18-29	23-0470-10-02	47 ohm RESISTOR (TAPE)
	V23-0470-10-00	47-ohm RESISTOR
R32	23-0222-10-02	2K2 ohm RESISTOR (TAPE)
	V23-0222-10-02	2K2 ohm RESISTOR
C1,3-5,88,110	22-1470-21-71	47 UF 16V ELEC CAP
	V22-1470-21-03	47 UF 16V ELEC CAP
	V22-1470-21-11	47 UF 16V ELEC CAP
	V22-1470-21-16	47 UF 16V ELEC CAP
	V22-1470-21-51	47 UF 16V ELEC CAP
C20-22,24,26-30, 32,34-36,38-42, 44,47,48,50,51, 53-57,59-64, 68-76,79-87, 90-98,101-109, 112-120,122,123	22-3473-18-Y2	0.047 UF 25V CER CAP
	V22-3473-18-15	0.147 UF 25V CER CAP
C18,46,52,66,77, 99,121	22-1101-11-71	100 UF 10V ELEC CAP
	V22-1101-11-03	100 UF 10V ELEC CAP
	V22-1101-11-55	100 UF 10V ELEC CAP
	V22-1101-11-56	100 UF 10V ELEC CAP
	V22-1101-11-58	100 UF 10V ELEC CAP
	A22-1101-21-02	100 UF 16V ELEC CAP
C23,25,45	22-3101-26-00	100 PF 50V ELEC CAP
	V22-3101-26-65	100 PF 50V ELEC CAP

DESTINATION	PART NUMBER	DESCRIPTION (continued)
C14,15,17	22-3102-28-00	1000PF 50V CER CAP
	A22-3102-26-00	1000PF 50V CER CAP
	A22-3102-28-15	1000PF 50V CER CAP
C16,19,33,37	22-1100-21-71	10 UF 16V ELEC CAP
	V22-1100-21-03	10 UF 16V ELEC CAP
	V22-1100-21-00	10 UF 16V ELEC CAP
C31	22-3180-26-00	18 PF 50V CER CAP
C43,49,58,65,67, 78,89,100,11	22-3470-26-00	47 PF 50V CER CAP
	A22-3470-25-00	47 PF 50V CER CAP
	V22-3470-26-01	47 PF 50V CER CAP
	V22-3470-26-65	47 PF 50V CER CAP
VC1,2	22-7002-01-00	4-20 PF TRIMMER CAP
	A22-7002-00-12	4-20 PF TRIMMER CAP
XTAL1	25-3015-02-00	14.31818 MHZ CRYSTAL
	A25-3015-00-04	14.31818 MHZ CRYSTAL
	A25-3015-00-00	14.31818 MHZ CRYSTAL
XTAL2	25-3063-00-01	30MHZ CRYSTAL
	V25-3063-00-00	30MHZ CRYSTAL
	A25-3061-00-01	30MHZ CRYSTAL
	A25-3061-00-02	30MHZ CRYSTAL
L1,2,4	25-1109-00-00	3 1/2T FERRITE BEAD CHOKE
L3,5,6,7	25-1020-00-00	3.3UH CHIKE COIL
D1-17	21-0001-00-00	IN4148 DIODE
Q1	20-0028-04-00	NA31 X I/J/H TRANSISTOR
	A20-0028-02-00	NA31 X J TRANSISTOR
SW1	42-0055-00-06	8 POLES DIP SWITCH
	V42-0055-00-00	8 POLES DIP SWITCH
	V42-0055-00-04	8 POLES DIP SWITCH
	V42-0055-00-07	8 POLES DIP SWITCH
SW2	42-0050-00-02	4 POLES DIP SWITCH
	V42-0050-00-04	4 POLES DIP SWITCH
JP3	40-0150-00-01	2 PINS CONNECTOR WAFER (WITH LOCK)
	V40-0150-00-00	2 PINS CONNECTOR WAFER (WITH LOCK)
JP5	40-0215-00-01	3 PINS WAFER
	V40-0215-00-00	3 PINS WAFER

DESTINATION	PART NUMBER	DESCRIPTION (continued)
J1-8	40-0608-62-01	62 PINS EDGE CONNECTOR
	A40-0618-62-01	62 POS EDGECARD CONNNECTOR
	A40-0472-00-00	62 WAYS PCB EDGE CONNECTOR
	A40-0608-62-03	62 PINS EDGE CONNECTOR
	V40-0608-62-02	62 PINS EDGE CONNECTOR
J9	40-0459-05-00	5 PINS DIN SOCKET
J10	40-0500-12-00	HEADER WITH LOCK
J11	40-0118-00-01	2 PINS CONNECTOR WAFER (RIGHT ANGLE)
	V40-0118-00-00	2 PINS CONNECTOR WAFER (RIGHT ANGLE)
J12	40-0120-00-01	5 PINS CONNECTOR WAFER (RIGHT ANGLE)
	V40-0120-00-00	5 PINS CONNECTOR WAFER (RIGHT ANGLE)

Note: *'A' placed before a part number indicates an alternative source.*

'V' placed before a part number indicates an alternative vendor.

LASER XT SERIES

PERSONAL COMPUTER

Technical Reference Manual

For LASER Multi-I/O Card

TABLE OF CONTENT

APPENDIX

CHAPTER 1

INTRODUCTION

1. INTRODUCTION

The Multi-I/O Card is a multifunction enhancement product for the IBM®PC,PC/XT family or compatible computers. This card incorporates Very Large Scale Integration (VLSI) Gate Array technology to reduce PCB area, minimize power consumption and improve reliability.

1.1 FEATURES AND AVAILABLE OPTIONS

The Multi-I/O Card provides standard features including:

- **Floppy disk interface**

  Two double-sided, double-density floppy disk drives are supported.

- **Parallel printer port**

  Interfaces with a Centronics type parallel printer.

- **RS-232C serial interface ports**

  Up to two RS-232C serial interface ports are provided for interfacing with modem, serial printer, remote display terminal or other serial devices.

- **Real - Time Clock**

  With the rechargeable backup battery, the real-time clock allows automatic setting up of time and date every time the computer is turned on.

- **Game Port**

  Connects to game paddle or joystick, for interactive games and graphics software.

- **Diskette Backup (Transcopy) Function**

  Provides diskette duplication of copy-protected or non-copy-protected software. This function is activated via jumper setting and an optional software package. Check with your dealer for details of this software.

The Multi-I/O Card is available in different versions for various levels of system requirements. Some version comes with only one serial interface port. Sockets and connectors are provided to allow upgrading to two serial ports. Refer to the user's manual for details of upgrading to two serial ports.

Another version of this card contains no floppy disk interface. This version is applicable to PC, PC/XT or compatible main units with built-in Floppy Disk Adapter logic.

Newer version (Enhanced) of this card has on board jumpers which allows disabling of some I/O functions when there is conflict with other devices in the system.

1.2 SYSTEM USAGE

The Multi-I/O Card interfaces with a PC, PC/XT or compatible main unit via a 62 pins PCB edge connector (slot). The following I/O Channel lines are used:

A0-A10	Address lines
D0-D7	Data lines
IOR, IOW	I/O Read and I/O Write lines
AEN	Address enable line
TC	Terminal count for DMA operation

RESET DRV	System Reset line
DACK 2	DMA acknowledge for DMA channel 2
DRQ 2	DMA request for DMA channel 2
IRQ2, IRQ3, IRQ4, IRQ5, IRQ6, IRQ7	Interrupt request levels 2,3,4,5,6 and 7
+5V, +12V, -12V	+5V, +12V and -12V DC supply voltages

The following table summarizes the I/O Address, Interrupt Levels and DMA Channels used by each of the functions:

Function	I/O Address (Hex)	Interrupt Level	DMA Channel
Floppy Disk Interface	3F2-3F5	6	2
Parallel Printer Port	378-37A or 3BC-3BE	7	/
RS232C Serial Port (COM1)	3F8-3FF	4	/
RS232C Serial Port (COM2)	2F8-2FF	3	/
Game Port	201	/	/
Real-Time Clock	340-35F or 2C0-2DF	2 or 5	/
Transcopy Function	66F or 6EF or 76F or 7EF	/	2

CHAPTER 2

BOARD LAYOUT, CONNECTORS AND JUMPERS

2. BOARD LAYOUT, CONNECTORS AND JUMPERS

The Multi-I/O Card occupies one 62 pins PCB edge connector (slot) as a typical long card does. However, the two RS232C Serial Interface Ports uses two additional brackets on the back panel of the computer main unit. Therefore, a total of three slots will be required.

2.1 BOARD LAYOUT

The following figure shows the major elements, in particular, the jumper blocks and connectors on the Multi-I/O Card.

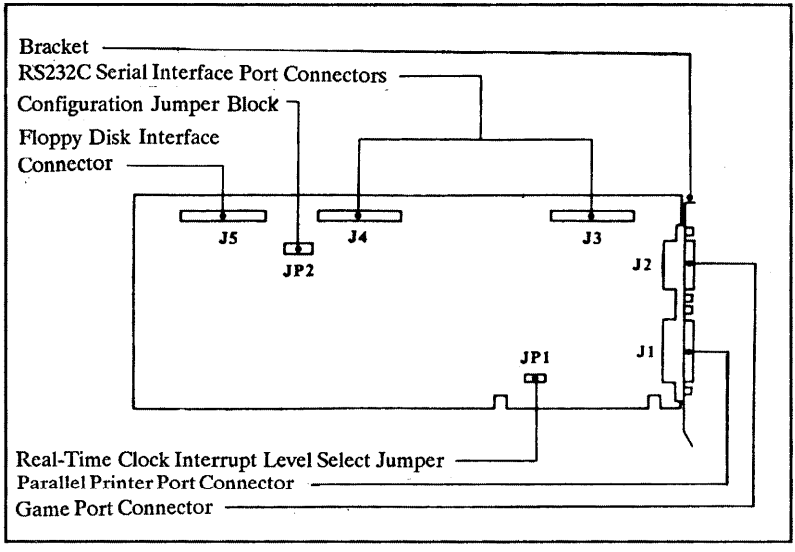


Fig. 2.1 Multi-I/O Board Layout

2.2 CONNECTORS AND JUMPERS

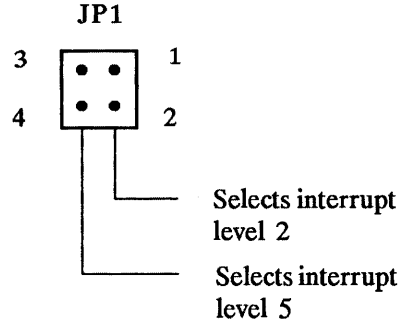
- Connector J1, a 25 pins "D" type female connector, is for connecting to a Centronics standard parallel printer.

- Connector J2, a 15 pins "D" type female connector, is for connecting to a joystick or game paddles.

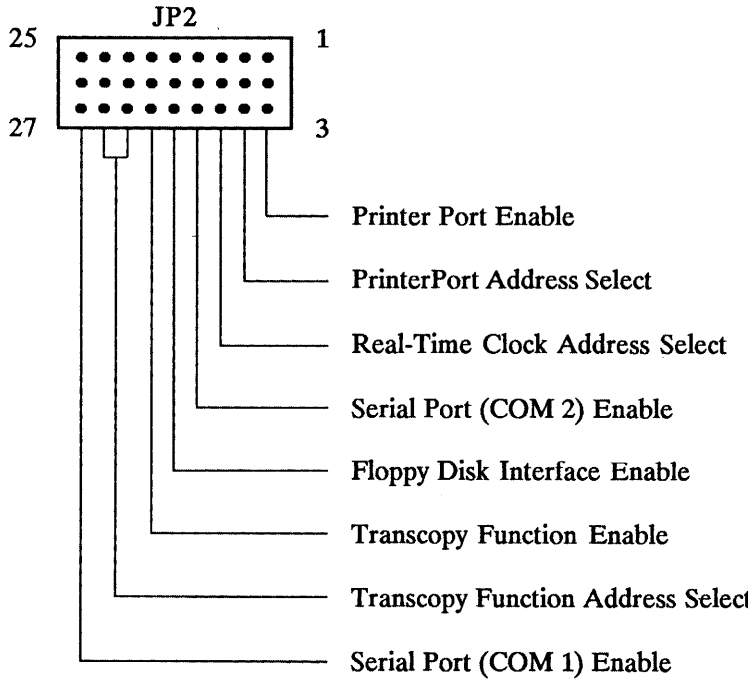
- Connectors J3 and J4, 26 ways header wafer connectors, are connectors of the two RS232C Serial Interface Ports. J3 is for the Primary Port (COM1) and J4 is for the Secondary Port (COM2). The signals on these connectors are carried to the back of the computers via the cable(s) supplied.

- Connector J5, a 34 ways header wafer connector, is for connecting to floppy disk drives.

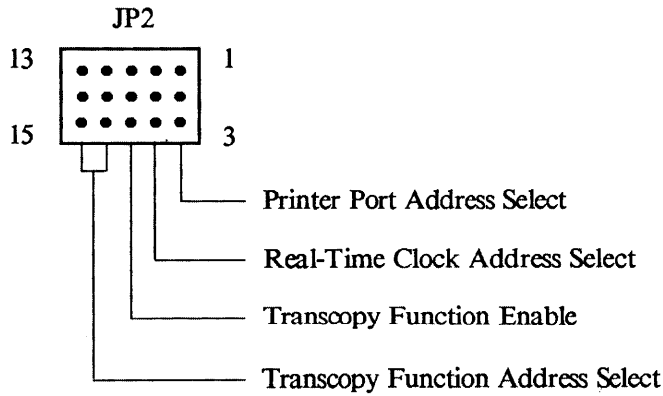
- JP1, a 4 pins jumper block, is for selecting the two different interrupt request levels for the Real-Time Clock.



JP2, a 27 pins jumper block on newer versions of the card, is a configuration Jumper Block which allows the user to select different addresses for some of the I/O functions. Moreover, some I/O functions can be disabled in case of address conflict with other devices in the system.



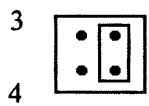
On some earlier version of the Multi-I/O Card, JP2 is a 15 pins jumper block which serves similar purpose as that on the newer version. The Floppy Disk Interface, Parallel Port, RS232C Serial Interface Ports are hardwired to be enabled.



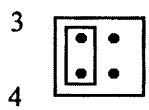
2.3 JUMPER SETTINGS

Various combinations of the jumper block and their meanings are summarized as follows. The jumpers irrelevant to the function under consideration are omitted for clarity.

Jumper Block JP1

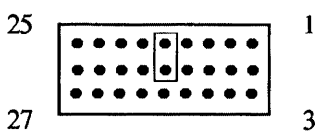


Selects Interrupt Level 2

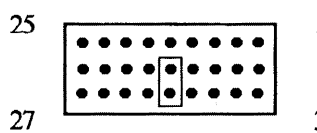


Selects Interrupt Level 5

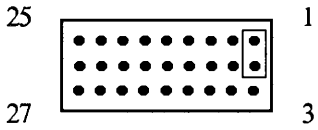
Jumper Block JP2 (on newer versions)



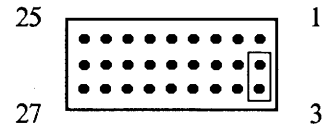
Floppy Disk
Interface Disabled



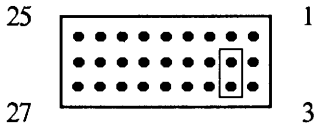
Floppy Disk
Interface Enabled



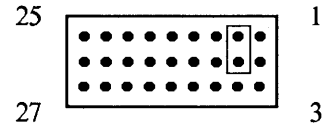
Parallel Printer
Port Disabled



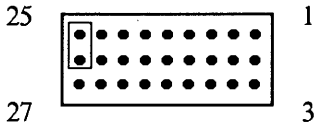
Parallel Printer
Port Enabled



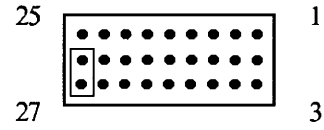
Printer Port
Address = 378-37A
(Hex)



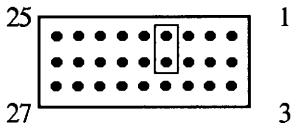
Printer Port
Address = 3BC-3BE
(Hex)



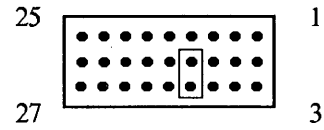
Serial Port (COM 1)
Disabled



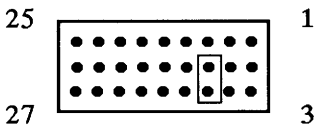
Serial Port (COM1)
Enabled



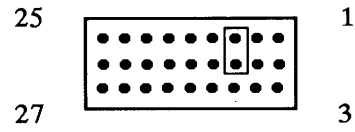
Serial Port (COM2)
Disabled



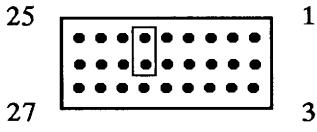
Serial Port (COM2)
Enabled



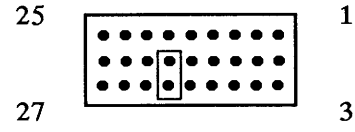
Select Real-Time Clock
Address = 340-35F (Hex)



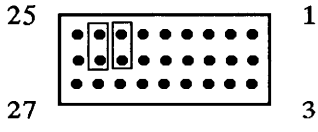
Select Real-Time Clock
Address = 2C0-2DF (Hex)



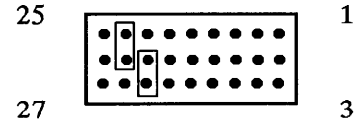
Transcopy Function
Disabled



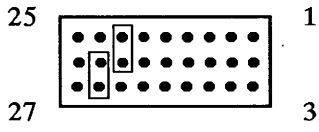
Transcopy Function
Enabled



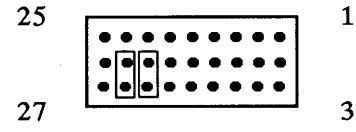
Transcopy Function
Address = 7EF (Hex)



Transcopy Function
Address = 76F (Hex)

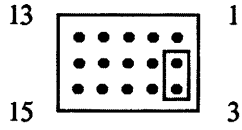


Transcopy Function
Address = 6EF (Hex)

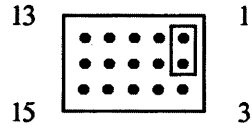


Transcopy Function
Address = 66F (Hex)

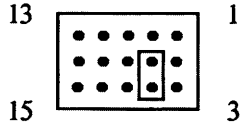
Jumper Block JP2 (on earlier version)



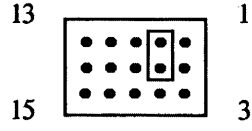
Printer Port
Address=378-37A (Hex)



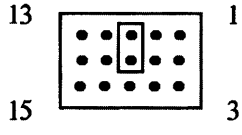
Printer Port
Address=3BC-3BE (Hex)



Select Real-Time Clock
Address=340-35F (Hex)



Select Real-Time Clock
Address=2C0-2DE (Hex)



Transcopy Function
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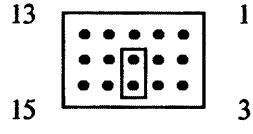
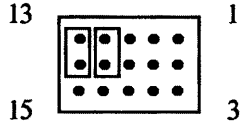
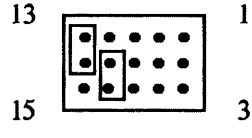


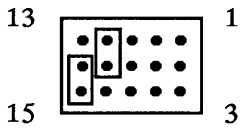
Transcopy Function
Enabled



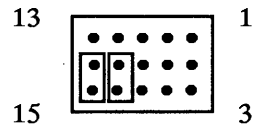
Transcopy Function
Address=7EF (Hex)



Transcopy Function
Address=76F (Hex)



Transcopy Function
Address=6EF (Hex)



Transcopy Function
Address=66F(Hex)

CHAPTER 3

HARDWARE DESCRIPTION

3. HARDWARE DESCRIPTION

This chapter describes the hardware structure of the Multi-I/O Card in terms of each function available. For a detail circuit diagram, component layout and component location list, please refer to the Appendix.

3.1 OVERALL BLOCK DIAGRAM

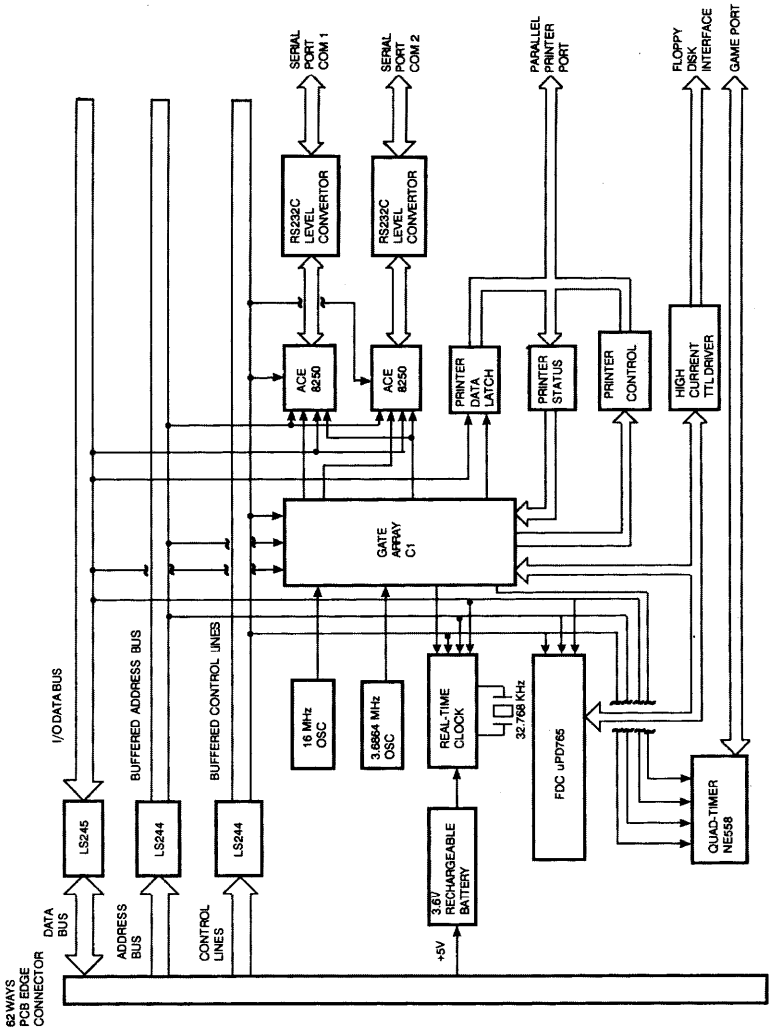


Fig . 3.1 Overall structure

The heart of the Multi-I/O Card is a 100 pins flat package Very Large Scale Integration (VLSI) Gate Array C1 (C1 is the code name used by the manufacturer for this particular chip and it will be used throughout this document).

The Gate Array C1 incorporates the hardware logic of :

- Floppy disk interface support logic for the external Floppy Disk Controller Chip uPD765 or compatibles.
- One Centronics Parallel Printer Interface.
- Address decoder and clock generator for two RS232C Serial Ports.
- Address decoder for Joystick/Game Port.
- Address decoder for Real-Time Clock chip.
- Logic for backup of protected floppy diskette (Transcopy Function).

Complete functions on the Multi-I/O Card are formed by addition of external LSI chips, buffers, latches, clock generators, battery and the required connectors.

Please refer to Chapter 4 for a complete specification of the Gate Array C1.

3.2 FLOPPY DISK INTERFACE AND TRANSCOPY FUNCTION

The floppy disk interface on the Multi-I/O Card is designed for double-sided, double-density, MFM-coded floppy disk drive. Up to two 5-1/4" double-sided, double-density floppy disk drives are supported. 3-1/2", 720K, double-sided disk drives with the same data rate and suitable device driver program will also work with the Multi-I/O Card.

3.2.1 Hardware

The floppy disk interface section includes a Floppy Disk Controller (FDC) chip uPD765, several high current TTL drivers and some logic circuitry inside the Gate Array C1. The following block diagram illustrates the structure.

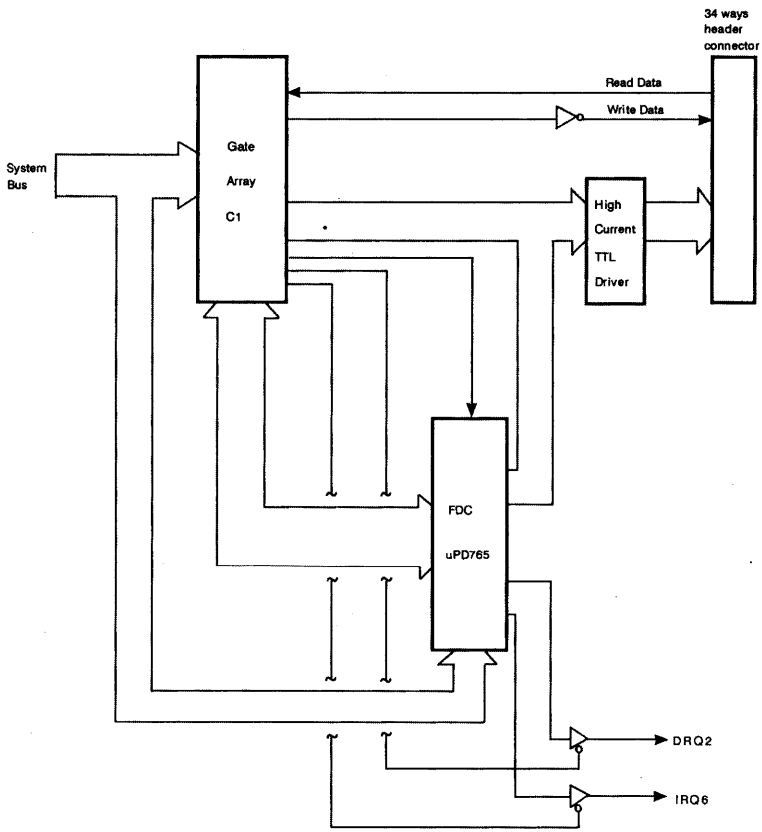


Fig. 3-2 Floppy Disk Interface

The disk drive parameters of the NEC uPD765 or compatible FDC are programmable. Transfer of data between the system memory and floppy disk controller is accomplished by Direct Memory Access (DMA) channel 2. An interrupt level 6 is also used to indicate when an operation is completed and a status condition requires processor attention.

The floppy disk interface employs write precompensation for its record data to improve reliability. Write pre-compensation is controlled by the FDC (uPD765) and performed inside the Gate Array C1. Write pre-compensation constant of 250ns using a 4MHz clock is implemented.

Data recovery of the MFM raw read data from floppy disk drive is done by a digital data separator built inside the Gate Array C1. The digital data separator is a synchronous counter type employing a 16MHz reference clock for higher reliability margin in the separated data.

The hardware logic of Transcopy is built entirely inside the Gate Array C1. This part includes a control port, serial to parallel convertor, parallel to serial convertor, status port, data / clock pulse generator and their associated address decoder. When the Transcopy function is activated via proper software, the reading / writing of floppy disk data will go directly through the Transcopy logic and the FDC uPD765 is bypassed. This enables the Transcopy function to resolve the copy-protection schemes used by most software packages. The Transcopy logic uses DMA channel 2 for its operation.

3.2.2 Programming Considerations

The floppy disk interface presents a high level command interface to software I/O drivers. From a programming point of view, the interface consist of an 8-bit digital-output register plus a uPD765 or compatible floppy disk controller. The following table shows the I/O Address used.

Register	I/O Address Used (Hex)
FDC Data Register	3F5
FDC Main Status Register	3F4
Digital Output Register	3F2

The floppy disk controller (FDC) contains two registers that may be accessed by the system processor: a status register and a data register. The 8-bit main status register contains the status information of the FDC and may be accessed at any time. The 8-bit data register stores data, commands, parameters, and provides floppy drive status information.

The FDC is capable of executing 15 different commands, each initiated by a multi-byte transfer from the processor. The results of command execution is also a multi-byte transfer back to the processor. Each command can be broadly divided into three phases:

- Command Phase
- Execution Phase
- Result Phase

Please refer to the data sheet of FDC uPD765 in the Appendix for details of these command descriptions.

The digital output register (3F2) is an output-only register used to control drive motors, drive selection and feature enable. All bits are cleared by the I/O interface reset line. The hardware logic for this register, together with other address decoding and DMA support logic, are all built inside the Gate Array C1.

The bits in the digital output register have the following functions:

Bits 0,1 Decoded by hardware to select one drive.

Bit 1	Bit 0	Drive Selected
0	0	0 (A)
0	1	1 (B)
1	0	Not applicable
1	1	Not applicable

Bit 2 The FDC (uPD765) is reset when this bit is clear. It must be set by program to enable the FDC.

Bit 3 This bit, when set, allows the FDC interrupt and DMA request to be gated onto the System Bus. When cleared, interrupt and DMA cannot be generated.

Bit 4,5 These bits controls, respectively, the spindle motors of drive 0 (A) and 1 (B). If they are set while the associated drive is selected, that motor will be turned on. Otherwise, it is off.

Bit 6, 7 Not used.

The Transcopy hardware appears to the programmer as a single Read/Write I/O port. The address of this I/O port is 7EF/76F/6EF/66F depending on the current jumper block settings.

Bit definitions are as follows:

When CPU write:

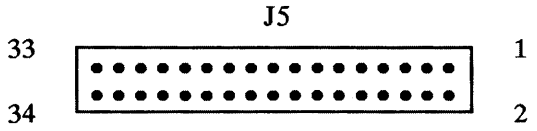
Bit 0	Transcopy DMA (channel 2) enable.
Bit 1	Transcopy Read control.
Bit 2	Transcopy Write control.
Bits 3,4,5	Internal Counter control.
Bits 6,7	Transcopy Data Rate control.

When CPU read:

Bits 0-5	Not used (garbage).
Bit 6	Value of Bit 7 on a previous CPU write operation to this I/O port.
Bit 7	Index signal from floppy disk drive.

All bits are cleared by system reset.

3.2.3 Connector Pin Assignment



Pin No.	Function
1-33 (odd no.)	Ground
2,4,6,34	Unused
8	Index
10	Motor Enable A
12	Drive Select B
14	Drive Select A
16	Motor Enable B
18	Direction (Stepper Motor)
20	Step Pulse
22	Write Data
24	Write Enable
26	Track 0
28	Write Protect
30	Read Data
32	Select Head 1

3.3 PARALLEL PRINTER PORT

The parallel printer port on the Multi-I/O card is a Centronics type parallel port. This type of parallel port can be used as a general input / output port for any device or application that matches its signal input / output specification.

3.3.1 Hardware

Functional block diagram of the parallel printer port is as follows:

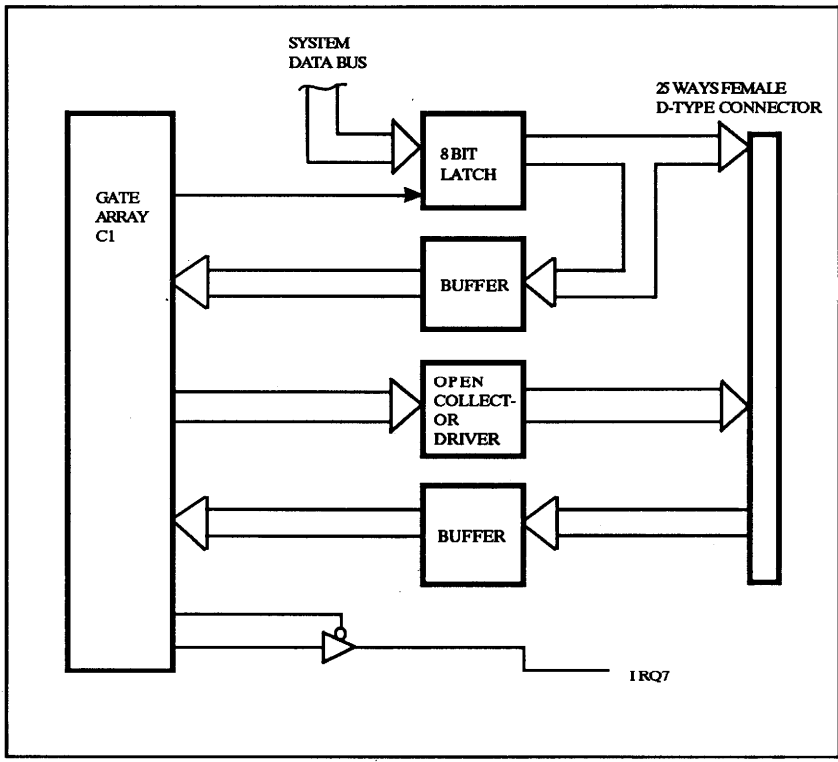


Fig. 3.3 Parallel Printer Port

8 bit data are output to the parallel device by writing to an 8-bit register, while status signals can be read through a status register. An input line (ACK) can be used to create an interrupt to the processor when it is properly enabled.

Most of the necessary hardware logic and decoding are built inside the Gate Array C1. Externally, an 8-bit data latch, which also serves as signal driver, plus some open collector drivers and buffer, are needed.

3.3.2 Programming Considerations

The parallel printer port uses I/O Address 378-37A (Hex) or 3BC-3BE (Hex), depending on the current jumper block setting. The hardware appears as registers / latches accessible by the system processor.

I/O Address (Hex)	Function
378/3BC	Printer Data Port
379/3BD	Printer Status Port
37A/3BE	Printer Control Port

Parallel Data Port 378 / 3BC:

This is an 8-bit read/write parallel data port for the parallel external device. The signal is held stable by latches and can be read back any time via the same I/O Address.

Printer Status Port 379 / 3BD:

This is a read only status port which can be accessed by the CPU to check for status of the external parallel device.

Bit Number	Status
0	Not used
1	Not used
2	Not used
3	Not used
4	SLCT
5	PE
6	ACK
7	BUSY

Printer Control Port 37A / 3BE:

The Printer control port, when written to, presents the following latched control signals to the external parallel device:

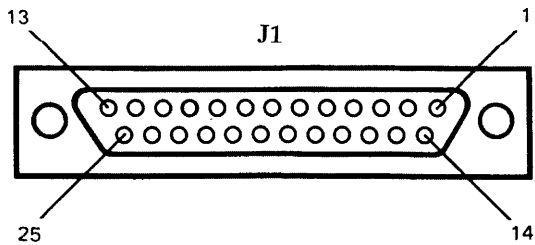
Bit Number	Control Signal
0	$\overline{\text{STROBE}}$
1	$\overline{\text{AUTO FD}}$
2	$\overline{\text{INIT}}$
3	$\overline{\text{SLCTIN}}$
4	IRQ7 Enable
5	Not used
6	Not used
7	Not used

The status of the control signals output being latched by a previous write command to I/O port 37A/3BE, can be read from the same address.

Bit Number	Status of Control Signal
0	$\overline{\text{STROBE}}$
1	$\overline{\text{AUTOFD}}$
2	$\overline{\text{INIT}}$
3	$\overline{\text{SLCTIN}}$
4	Not used
5	Not used
6	Not used
7	Not used

System interrupt level 7 can be enabled by setting bit 4 in the Printer Control Port (37A / 3BE) and activating the $\overline{\text{ACK}}$ input line.

3.3.3 Connector Pin Assignment

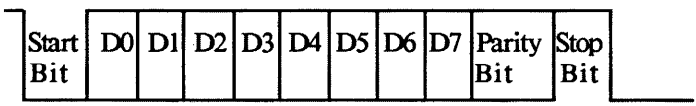


Pin No	Function
1	$\overline{\text{STROBE}}$
2	Parallel Data D0
3	Parallel Data D1
4	Parallel Data D2
5	Parallel Data D3
6	Parallel Data D4
7	Parallel Data D5
8	Parallel Data D6
9	Parallel Data D7
10	$\overline{\text{ACK}}$
11	BUSY
12	PE
13	$\overline{\text{SLCT}}$
14	$\overline{\text{AUTO FD}}$
15	$\overline{\text{ERROR}}$
16	$\overline{\text{INIT}}$
17	$\overline{\text{SLCTIN}}$
18-25	GROUND

3.4 RS232C SERIAL INTERFACE PORTS

The Multi-I/O card supports up to two RS232C Serial Interface Ports. They are designated as COM1 and COM2 in accordance with their I/O Address 3F8-3FF (Hex) and 2F8-2FF (Hex) respectively. These serial ports provide interface for serial devices including modem, serial printer and terminal.

The serial communication ports are fully programmable and supports asynchronous communications only. They add and remove start bits, stop bits and parity bits. A programmable baud rate generator allows operation from 50 baud to 9600 baud. Five, six, seven or eight bit characters with 1, 1-1/2 or 2 stop bits are supported.



Each serial port has it assigned level of system interrupt. A fully prioritized interrupt system within each serial port controls transmit, receive, error, line status and data set interrupts. Diagnostic capabilities provide loopback functions of transmit / receive and input / output signals.

3.4.1 Hardware Description

Following is a block diagram of hardware for one serial port (COM1).

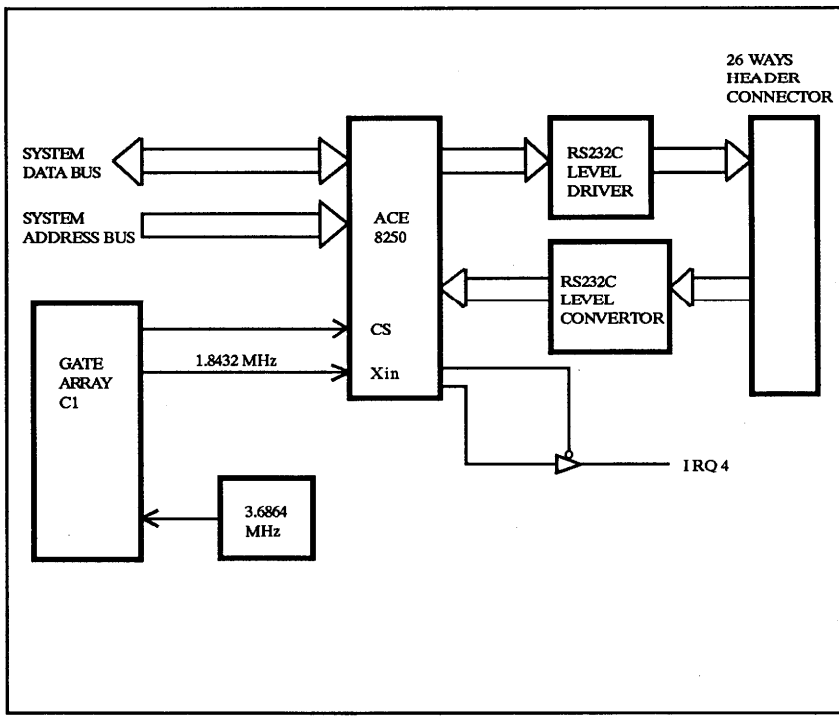


Fig. 3.4 RS232C Serial Interface Port

The heart of the Serial Communication Port is the INS8250 Asynchronous Communication Element (ACE), or its functional equivalent . Address decoding and clock generation is done in Gate Array C1. A 3.6864MHz signal input to Gate Array C1 is divided by two and fed to the INS8250 ACE chip as a 1.8432 MHz master clock. Baud rates of 50 to 9600 are generated from this 1.8432 MHz signal.

The serial data output, together with modem control output from the ACE, are changed from TTL voltage into RS232C voltage levels via signal drivers 1488 or equivalent. Conversely, RS232C voltage levels are converted back to TTL levels by signal converters 1489 or equivalent and fed to the ACE inputs.

3.4.2 Programming Considerations

Apart from the general function listed above, the ACE also features:

- Full double buffering eliminates extra hardware / software for precise synchronization.
- Modem control functions of Clear to Send (CTS), Request to Send (RTS), Data Set Ready (DSR), Data Terminal Ready (DTR), Ring Indicator (RI), and Carrier Detect.
- False - start bit detection.
- Line - break generation and detection.

The INS8250 ACE is fully programmable for each function and any communication protocol must be loaded before the serial port is operational. This is done by selecting the proper I/O Address for each Serial Port. The following tables summarizes the I/O Address assigned to the internal registers of INS8250 ACE in the Multi-I/O card. The divisor latch access bit DLAB (bit7) of the line control register is used to select certain register.

I/O Decode (in Hex)		Register Selected	DLAB State
COM1	COM2		
3F8	2F8	TX Buffer	DLAB=0(Write)
3F8	2F8	RX Buffer	DLAB=0(Read)
3F8	2F8	Divisor Latch LSB	DLAB=1
3F9	2F9	Divisor Latch MSB	DLAB=1
3F9	2F9	Interrupt Enable Register	
3FA	2FA	Interrupt Identification Registers	
3FB	2FB	Line Control Register	
3FC	2FC	Modem Control Register	
3FD	2FD	Line Status Register	
3FE	2FE	Modem Status Register	

I/O Decodes

Hex Address 3F8 to 3FF and 2F8 to 2FF											
A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	DLAB	Register
1	1/0	1	1	1	1	1	X	X	X		
							0	0	0	0	Receive Buffer (read) Transmit Holding Reg (write)
							0	0	1	0	Interrupt Enable
							0	1	0	X	Interrupt Identification
							0	1	1	X	Line Control
							1	0	0	X	Modem Control
							1	0	1	X	Line Status
							1	1	0	X	Modem Status
							1	1	1	X	None
							0	0	0	1	Divisor Latch (LSB)
							0	0	1	1	Divisor Latch (MSB)

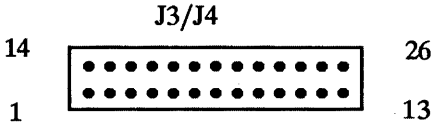
Address Bits

Note: Bit 8 will be logical 1 for the port designated as COM1 or a logical 0 for the port designated as COM2.

A2, A1 and A0 bits are used to select the different register of the communications chip.

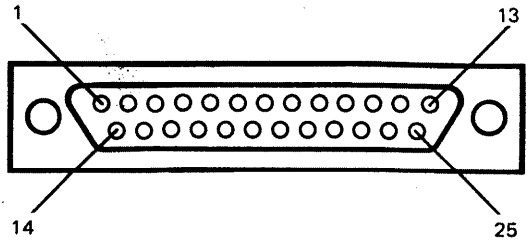
Please refer to the data sheet of ACE INS8250 in the Appendix for details of these internal registers.

3.4.3 Connector Pin Assignment



Pin No.	Function
1	Ground
2	TX
3	RX
4	RTS
5	CTS
6	DSR
7	Ground
8	RLSD
9-19	Not used
20	DTR
21	Not used
22	RI
23-26	Not used

DB25 male connector on bracket



Pin No.	Function
1	Ground
2	TX
3	RX
4	RTS
5	CTS
6	DSR
7	Ground
8	RLSD
9-19	Not used
20	DTR
21	Not used
22	RI
23-25	Not used

3.5 GAME PORT

The Game Port on the Multi-I/O Card allows up to four game paddles or two joysticks to be attached. In addition, inputs for four switch buttons are provided. Paddle and joystick positions are determined by the variable resistance values sensed by the Joystick/ Game Port. The real-time resistive values are converted into a relative paddle or joystick position via appropriate software.

3.5.1 Hardware

The following is the block diagram of the joystick / game port.

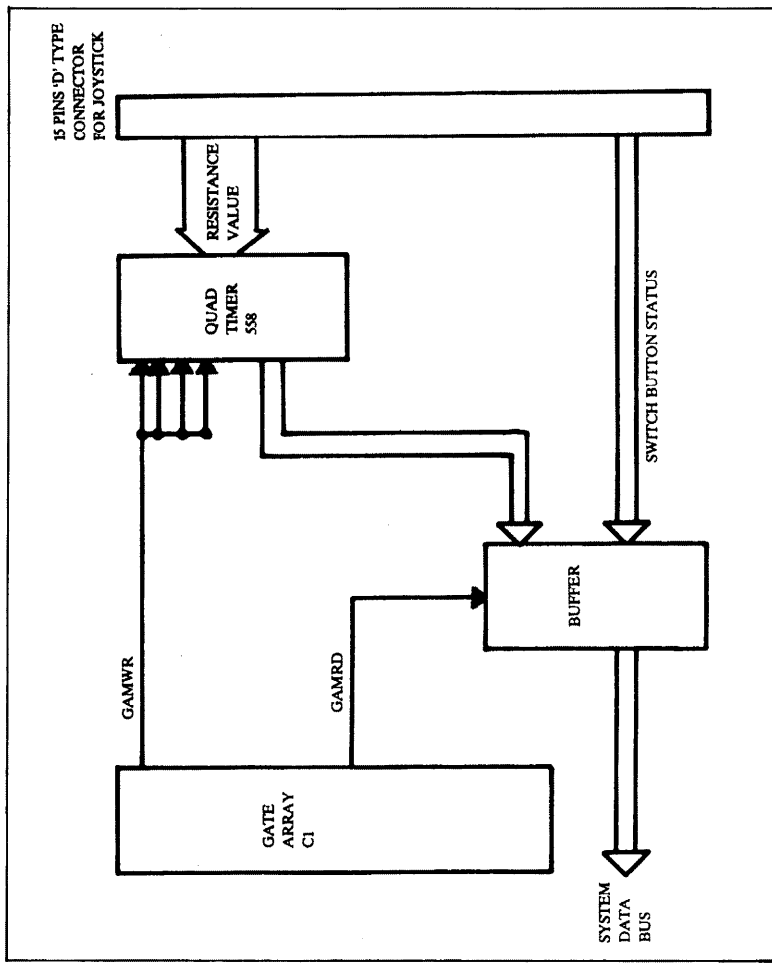


Fig. 3.5 Joystick/Game Port

The chip for conversion of resistance value into digital state is the Quad-Timer NE558 or equivalent. Address decoding for the Joystick / Game Port is provided by the Gate Array C1. I/O Address

for triggering of four monostable timers as well as reading of position / button status byte is 201 Hex. The position/button status are gated via data buffer with its enable line decoded from Gate Array C1.

3.5.2 Programming Considerations

The Joystick / Game Port appears to the programmer as one Read/ Write Port with I/O Address 201 Hex.

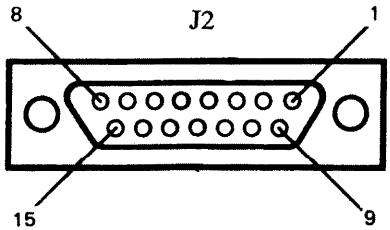
When an I/O write command is issued to port address 201 Hex, irrespective of the data written, all four monostable outputs go high and will remain high for varying periods of time depending on the position each variable resistor of the joystick is set. The variable resistance on the joystick should have a range from 0 to 100K-ohms.

These four monostable timer outputs are read by an I/O read command from port address 201 Hex and are reflected on data bits 0 through 3.

Bit 4 through 7 of the I/O port reflects the real-time status of the switch buttons. These buttons default to an open state and are read as "1". When a button is pressed, it is read as "0:". Programmers should note that these buttons are not debounced by hardware.

Bit Number	Function
0	Position 0
1	Position 1
2	Position 2
3	Position 3
4	Switch Button 0
5	Switch Button 1
6	Switch Button 2
7	Switch Button 3

3.5.3 Connector Pin Assignment



Pin No.	Function
1	+5V DC
2	Button 0
3	Position 0
4	Ground
5	Ground
6	Position 1
7	Button 1
8	+5V DC
9	+5V DC
10	Button 2
11	Position 2
12	Ground
13	Position 3
14	Button 3
15	+5V DC

3.6 REAL-TIME CLOCK

The Multi-I/O Card is equipped with a Real-Time Clock and re-chargeable battery backup. This function maintains the time and calendar, and, with suitable software, allows automatic setting up of time and date each time the computer is turned on.

3.6.1 HARDWARE

Following is a block diagram of the Real-Time Clock.

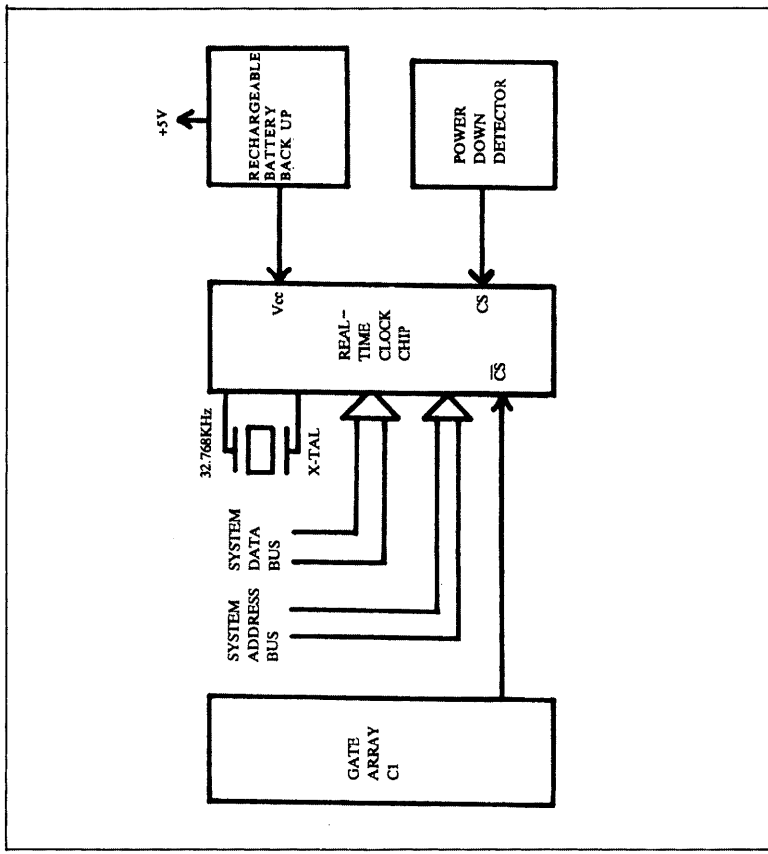


Fig. 3.6 Real-Time Clock

The heart of the Real-Time Clock is the real-time clock chip. The Multi-I/O Card has made provision to work with two different real-time clock chips, namely, the OKI MSM 6242 or the RICOH RP5C15. These chips are on different locations of the PCB.

The real-time clock chip runs with a clock of 32.768 KHz for its internal counting operation.

This chip normally draws power from the computer's +5V supply when the computer is turned ON. The backup battery is recharged from the +5V supply. When the power is OFF, the backup battery replaces the normal +5V to keep the chip running.

A power down detection circuitry is added to pull the CS line of the real-time clock chip to logic low as soon as the computer's +5V supply is dropping. This prevents transient garbage to be written to the chip during power down.

Address decoding for the real-time clock chip is done in Gate Array C1. The I/O Address range used is 340-35F (Hex) or 2C0 - 2DF (Hex), depending on the current jumper block setting.

3.6.2 Programming Considerations

The Real-Time Clock function appears to the programmer as a number of CPU addressable registers. These registers serve functions including second, minute, hour, day, month, year and days of the week.

The real-time clock chip incorporates 16 such registers, while the Gate Array C1 decodes 32 different addresses. The upper 16 addresses map to the lower 16 addresses.

The Real-Time Clock utility programs SETCLOCK,GETCLOCK supplied with the card automatically handle the different chips used and different addresses selected.

Refer to the Appendix for detail meaning of the real-time clock chip registers.

CHAPTER 4

GATE ARRAY C1

CHAPTER 4
GATE ARRAY C1

The Gate Array C1 is a 100 pins flat package VLSI Gate Array designed to implement a number of I/O functions for the IBM®PC, PC/XT and compatibles.

It consists of the logic circuitry for the following popular I/O features:

- Floppy disk interface support logic for the Floppy Disk Controller Chip uPD765.
- One Centronics Parallel Printer Interface.
- Address decoders for two RS232C Serial ports.
- Address decoder of a Joystick/Game Port
- Address decoder for a Real-Time Clock Chip.
- Logic circuitry for backup of copy-protected diskette (Transcopy Function).

4.1 FUNCTIONAL BLOCK DIAGRAM

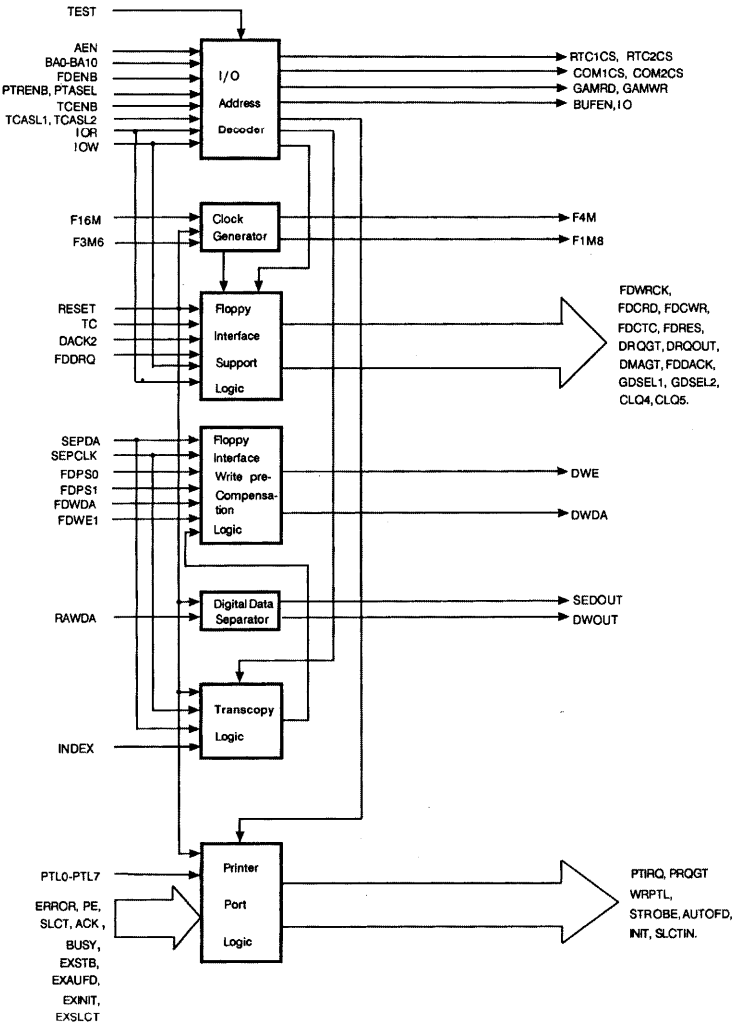


Fig 4.1 Gate Array C1 Function Diagram

4.2 PIN ASSIGNMENT AND SIGNAL DESCRIPTION

Abbreviation on pin type:

I	Input
O	Output
I/O	Bi-directional

Pin No.	Pin type	Name	Description
1	I	PTRENB	Printer Port enable line. Active high input. 1=printer port enabled 0=printer port disabled
2	I	PTASEL	Printer Port I/O address select. 1=378-37A (Hex) 0=3BC-3BF (Hex)
3	O	RTC1CS	Real-Time Clock 1 address decoder. Active low output. Address range=340-35F (Hex)
4	/	N.C.	No connection.
5	O	RTC2CS	Real-Time Clock 2 address decoder. Active low output. Address range=2C0-2DF (Hex)
6	O	COM1CS	RS232C Serial Port 1 address decoder. Active low output. Address range=3F8-3FF (Hex)
7	O	COM2CS	RS232C Serial Port 2 address decoder. Active low output. Address range=2F8-2FF (Hex)

8	I	FDENB	Floppy Disk Interface enable. Active low input. 0=Floppy Interface enabled 1=Floppy Interface disabled
9	I	TCENB	Transcopy Function enable. Active high input. 1=Transcopy Function enabled 0=Transcopy Function disabled
10	I	TCASL1	Transcopy Function address select 1.
11	I	TCASL2	Transcopy Function address select 2. Different combinations of TCASL1, TCASL2 results in one of four possible addresses for Transcopy Function:

TCASL2	TCASL1	I/O Address
0	0	7EF
0	1	76F
1	0	6EF
1	1	66F

12	I	F3M6	Input signal from an external 3.6864MHz oscillator. The signal is divided by 2 in Gate Array C1 to generate a 1.8432MHz output signal for the serial communication chips.
13	I	F16M	Input signal from an external 16MHz oscillator. All necessary timing signal for the Floppy Disk Interface are derived from this 16MHz signal.

14	O	GDSEL2	Partially decoded Drive B select signal for the Floppy Disk Interface. Active high output. This signal should be NAND with CLQ5 to produce the valid Drive B select signal.
15	/	GND	0 V
16	O	GDSEL1	Partially decoded Drive A select signal for the Floppy Disk Interface. Active high output. This signal should be NAND with CLQ4 to produce the valid Drive A select signal.
17	O	CLQ4	Motor enable signal for floppy disk drive A. Active high output.
18	O	CLQ5	Motor enable signal for floppy disk drive B. Active high output.
19	O	DWE	Floppy drive write enable signal. Active high output.
20	O	DWDA	Floppy drive write data signal. Active high output.
21	O	IO	This signal is a logical AND of the IOR, IOW. Active low output, indicating I/O Read, I/O Write is in progress.
22	O	F1M8	This signal is a 1.8432MHz square wave output signal derived from the 3.6864MHz input signal.

23	O	F4M	This is a 4MHz square wave output derived from the 16MHz input signal. This signal is used as the clock input of an external FDC uPD765, or as the reference clock in an external data separator WD9216.
24	O	FDCWR	Decoded output signal to the Write input of an external FDC uPD765. Active low output. This line is activated when the CPU writes to the FDC or DMA write to the FDC is in progress.
25	O	FDCRD	Decoded output signal to the Read input of an external FDC uPD765. Active low output. This line is activated when the CPU reads from the FDC or DMA read from the FDC is in progress.
26	O	FDCTC	Terminal count output to an external FDC uPD765. Active high output. This line is activated at the end of each DMA transfer for Floppy Disk Interface.
27	/	N.C.	No connection.
28	O	FDWRCK	Write clock output to an external FDC uPD765. 500 KHz positive going pulse signal.
29	O	FDRES	Reset output to an external FDC uPD765. Active high output. This line is activate when a "0" is written to the Digital Output Register (Hex 03F2) of the Floppy Disk Interface inside the Gate Array.

30	O	DRQGT	Control output for Floppy Disk Interface DMA Request. Active low output. This line is used for enabling an external tri-state buffer (LS125) which has output driving the system DMA Request channel 2.
31	O	DRQOUT	Floppy Disk Interface DMA Request. Normally tri-state with active high output. This line is connected to a tri-state buffer (LS125) which drives the system DMA Request channel 2.
32	O	DMAGT	Control output for Floppy Disk Interface Interrupt Request. Active low output. This line is used for enabling an external tri-state buffer (LS125) which has input from the uPD765 Interrupt line, and drive the system IRQ level 6.
33	I	FDPS0	Floppy Disk Interface Write Precomp 0.
34	I	FDPS1	Floppy Disk Interface Write Precomp 1. FDPS0,FDPS1 are input signals from an external FDC uPD765. These two signals controls the amount of write pre- compensation to be effected on the write data to floppy disk drive. Maximum write pre-compensation is +/-250nS.
35	I	TC	System Terminal Count. Active high input.
36	O	SEDOUT	Separated Data out. Active low output from an internal digital data separator inside the Gate Array. The active duration of the pulse output is 62.5nS.

37	O	DWOUT	Data Window out. This is a 250KHz rectangular wave output from the internal digital data separator inside the Gate Array. The phase (edges) of this signal will shift back and forth according to the raw read data from the floppy disk drive.
38	I	SEPDA	Separated Data input. This is the separated read data for use by Floppy Disk Interface and the Transcopy Function. If the internal digital data separator is used, this pin should be connected to the SEDOUT (pin 36) of the Gate Array. If an external data separator is adopted, this pin should be connected to the separated data output from the external data separator.
39	I	SEPCLK	Separated Clock input. This is the separated clock, or the data window used by the Floppy Disk Interface and the Transcopy Function. If the internal digital data separator is used, this pin should be connected to the DWOUT (pin 37) of the same Gate Array. If an external data separator is adopted, this pin should be connected to the separated clock, or data window output from the external data separator.
40	I	FDWE1	Floppy disk drive write enable. Active high input from an external FDC uPD765.
41	/	VCC	+5V DC supply voltage.
42	I	FDWDA	Floppy disk write data. Active high input from an external FDC uPD765. This write data is not yet write pre-compensated.

43	O	FDDACK	Floppy Disk Interface DMA Acknowledge. Active high output signal to an external FDC uPD765.
44	I	FDDRQ	Floppy Disk Interface DMA Request. Active high input signal from an external FDC uPD765.
45	I	RAWDA	Raw read data from floppy disk drive. Active low input which is used by the internal digital data separator.
46	O	PTIRQ	Printer Port interrupt request. Tri-state normally, high when active. This pin should connect to a tri-state buffer (LS125) which drives the system Interrupt level 7.
47	O	PRQGT	Printer Port interrupt request control. Active low output. This pin should be used for controlling a tri-state buffer (LS125) which drives the system Interrupt level 7.
48	I	ERROR	Printer status signal - ERROR.
49	I	INDEX	Floppy disk drive Index signal. Active low input. This signal is used by the Transcopy logic inside the Gate Array.
50	I/O	BD0	Data line D0
51	I/O	BD1	Data line D1
52	I/O	BD2	Data line D2
53	I/O	BD3	Data line D3

54	I/O	BD4	Data line D4
55	I/O	BD5	Data line D5
56	I/O	BD6	Data line D6
57	I/O	BD7	Data line D7
58	I	AEN	System Address Enable. Active low input. All CPU Read/Write takes place when AEN is active.
59	I	IOR	System I/O Read. Active low input.
60	I	IOW	System I/O Write. Active low input.
61	I	DACK2	System DMA channel 2 Acknowledge. Active low input.
62	I	RESET	System Reset. Active high input.
63	I	BA0	Address line A0
64	I	TEST	Test input for factory diagnostic purpose. Must be grounded (tie to 0 V) for normal operation.
65	/	GND	0 V
66	I	BA1	Address line A1
67	I	BA2	Address line A2
68	I	BA3	Address line A3
69	I	BA4	Address line A4
70	I	BA5	Address line A5
71	I	BA6	Address line A6

72	I	BA7	Address line A7
73	I	BA8	Address line A8
74	I	BA9	Address line A9
75	I	BA10	Address line A10
76	O	STROBE	Printer control output - STROBE
77	O	AUTOFD	Printer control output - AUTOFD
78	O	INIT	Printer control output - INIT
79	O	SLCT IN	Printer control output - SLCT IN
80	O	WRPTL	Printer Port parallel data latch signal. Active low output. Decoded address = 378/3BC (Hex)
81	I	PTL0	Printer Port parallel data 0 input
82	I	PTL1	Printer Port parallel data 1 input
83	I	PTL2	Printer Port parallel data 2 input
84	I	PTL3	Printer Port parallel data 3 input
85	I	PTL4	Printer Port parallel data 4 input
86	I	PTL5	Printer Port parallel data 5 input
87	I	PTL6	Printer Port parallel data 6 input
88	I	PTL7	Printer Port parallel data 7 input
89	O	BUFEN	Enable signal for an external data buffer (LS245) connected between the data lines of the Gate Array and the system data bus.
90	I	EXSTB	Printer status signal - STROBE
91	/	VCC	+5V DC supply voltage.
92	I	EXAUFD	Printer status signal - AUTOFD
93	I	EXINIT	Printer status signal - INIT

94	I	EXSLCT	Printer status signal - SLCT IN
95	I	SLCT	Printer status signal - SLCT
96	I	PE	Printer status signal - PE
97	I	ACK	Printer status signal - ACK
98	I	BUSY	Printer status signal - BUSY
99	O	GAMRD	Game Port Read signal. Active low output. I/O address decoded = 201 (Hex)
100	O	GAMWR	Game Port Timer Trigger. Active low output. I/O address decoded = 201 (Hex)

4.3 ELECTRICAL SPECIFICATIONS

4.3.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	Vcc	-0.3~+6.7	V
Terminal voltage	Vt	-0.3~Vcc+0.3	V
Output Current			
- per one output	Io	-8~+8	mA
- total	Iot	-40~+40	mA
Operating Temperature	Topr	-20~+75	C
Storage Temperature			
- with Bias	Tbias	-20~+85	C
- without Bias	Tstg	-55~+125	C

4.3.2 Electrical Characteristics

Vcc = 5V +/- 5%, Ta = -20°to 75°C

Parameter	Symbol	min	max	unit
Input Voltage	VIH	2.2	Vcc+0.3	V
	VIL	-0.3	0.8	V
Output Voltage	VOH	3.5		V
	(IOH = -2mA)			
	VOL		0.5	V
	(IOL = 5mA)			
Input Leakage Current	ILI		1	uA
Output Leakage Current	ILO		1	uA

4.4 MECHANICAL INFORMATION

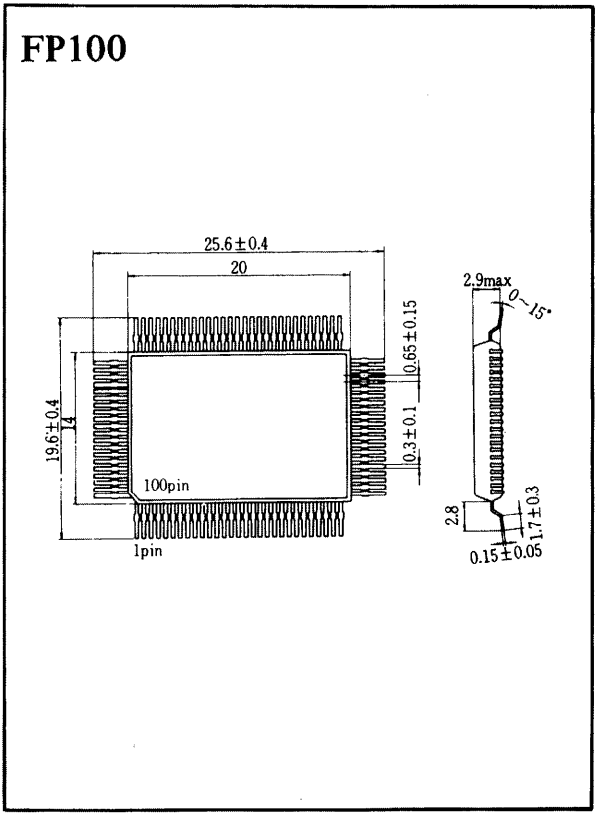


Fig 4.2 Gate Array C1

CHAPTER 5

TROUBLE - SHOOTING GUIDE

CHAPTER 5
TROUBLE-SHOOTING GUIDE

This chapter describes the general guidelines for trouble-shooting of the Multi-I/O Card.

For more detail information on logic states please refer to the Gate Array C1 Specification in Chapter 4, data sheets of various components and the circuit schematic diagrams in the Appendix.

Technical reference manual of the host main unit will also be of help.

Refer to your DOS (Disk Operating System) User's Manual for errors associated with disk I/O.

The description contained in this chapter assumes that the problem comes from, or most likely from, the Multi-I/O Card. This can easily be verified by removing the card from the system, exchange for another I/O Card, or move the suspected Multi-I/O Card to another system and observe the result. Remember to turn power OFF before removing any card.

5.1 GENERAL FAILURE

Symptom

Computer system no response after power up. Power indicator on main unit does not light up.

Possible causes	Solution
. +5V failure/ short circuited on Multi-I/O Card.	. Check for +5V DC short-circuiting on Multi-I/O Card
	. Check for short-circuited decoupling capacitor.
	. Check for short-circuited I.C. chips.
	. Check if the card is inserted properly in the main unit slot.

Symptom

Main unit power indicator lights up. Computer no video, or no other response, including the power up 'beep' sound.

Possible causes	Solution
. System address bus, data bus, or control lines contamination due to Multi-I/O Card failure.	. Check data buffer and address buffer I.C. U1,U6,U12 on Multi-I/O Card.
. Multi-I/O Card not inserted properly.	. Check if the card is inserted properly in the slot.

5.2 FLOPPY DISK INTERFACE/TRANSCOPY FAILURE

Symptom

Floppy drive not booting.

Possible causes	Solution
. Floppy drive function disabled (on newer versions of this card).	. Change jumper block setting to enable this function.
. I/O Address conflict with another floppy drive adapter on the main unit.	. Change jumper block setting to disable this function, while use the built-in adapter on the main unit.
. Data bus contamination on all I/O functions.	. Check I/O data bus buffer U1. . Check all other LSI, I.C. connected to the I/O data bus. . Check Gate Array C1 (U20).
. Floppy drive interface logic failure.	. Check FDC chip uPD765 (U27), U21,U25,U26, U30,U28,U29,U14,U30, R19,R20,R21,R22,Xtal 2.
. Floppy drive interface cable not properly connected.	. Check cables and connectors for proper connection and correct orientation.

. Floppy disk drive failure.	. Check for proper jumper (if any) settings on floppy disk drive. . Check power (DC +5V, +12V) on floppy disk drive.
. DIP switch on main unit set wrongly, which indicates no floppy disk drive.	. Check for proper DIP switch settings on main unit.

Symptom

Floppy drive boot up normal. Unable to format or write data to drive, or fail to retrieve the data written by the same computer.

Possible causes	Solution
. Floppy drive failure.	. Check floppy drive.
. Floppy drive interface write logic failure.	. Check Gate Array C1 (U28), uPD765 (U27), U29.
. Floppy write data Precompensation failure.	. Check Gate Array C1 (U28), uPD765 (U27).
. Floppy drive signal cable broken.	. Check for proper connecting cable between card and disk drive.
. Diskette defective or improper media quality.	. Check diskette for double-sided, double-density and it is not defective.

Symptom

Transcopy function not working. Floppy disk function normal.

Possible causes	Solution
. Transcopy function not enabled.	. Check jumper block for proper setting.
. Address conflict with other I/O devices on the system slot.	. Check for I/O devices attached to system slot. Select another I/O address for Transcopy in case of conflict.
. Transcopy logic failure.	. Replace Gate Array C1 (U20).

5.3 PARALLEL PRINTER PORT FAILURE

Symptom

Printer Port not functioning properly.

Possible causes	Solution
. Printer cable and connectors not properly connected.	. Check for proper connection between the card and printer.
. Printer port not enabled (on newer versions of the card)	. Change jumper block setting to enable function.
. Operating System is assumming another parallel port, with different address, on another peripheral card.	. Check for another parallel port in the system. Use the other port for printer if higher priority is given to that port.
. Printer port logic failure.	. Check Gate Array C1 (U20), U2,U8,U3,U7.
. Printer interrupt failure.	. Check printer port interrupt logic in Gate Array C1 (U20), U9.

5.4 RS232C SERIAL INTERFACE PORT FAILURE

Symptom

RS232C Serial Interface Ports not functioning properly.

Possible causes	Solution
. Serial cables and connectors not connected properly.	. Check for proper connection between card and bracket, between connectors and serial device.
. Serial Ports not enabled (on newer versions of the card).	. Change jumper block settings to enable the function.
. Only one serial port is built-in on some cards.	. Expand to two serial ports. Refer to user's manual.
. Improper serial cable used for serial printer (different from modem cables).	. Check if the proper serial printer cable is used.
. Serial port hardware logic failure.	. Check Gate Array C1 (U20), ACE 8250 (U15, U16), RS232 signal convertors U10, U11,U17,U18,U19,U9, Xtal 1.

5.5 GAME PORT FAILURE

Symptom

Game Port not functioning properly.

Possible causes	Solution
. Joystick/paddle connector or cable not properly connected,	. Check for proper connection in the cable and connector of joystick/paddle.
. Defective joystick or paddle.	. Check for defective joystick/paddle device, or improper resistance value inside joystick.
. Game port hardware logic failure.	. Check Gate Array C1(U20),U5,U4,R1-R4,C26-C29.

5.6 REAL-TIME CLOCK FAILURE

Symptom

Real -Time Clock not responding, or lose time after power down, or no alarm.

Possible causes	Solution
. Real-time clock not enabled.	. Check for proper jumper setting to enable the function.
. Defective real-time clock hardware logic.	. Check Gate Array C1(U20),U23(or U22), Xtal 3, VC1, C84,Q1,Q2,D1,D2 U21,U26.
. Defective battery or charging circuit.	. Check 3.6V battery, C83,R17,D3.
. Computer or card not used for too long a time, resulting in battery exhausted.	. Power up the computer a few hours to charge the battery.
. Address conflict with other devices in the system.	. Check for address conflict and change to another address for the real-time clock.

Z765A FDC
Floppy Disk Controller

Zilog

NEW 1985

Advance Information
Product
Specification

April 1985

FEATURES

Address Mark detection circuitry internal to the FDC simplifies the phase locked loop and read electronics. The track stepping rate, head load time, and head unload time are user-programmable.

Z765A features are:

- IBM-compatible format, Single and Double Density
- Multisector and multitrack transfer capability
- Data scan capability—scans a single sector or an entire cylinder comparing byte-for-byte host memory and disk data
- Drives up to 4 floppy-disk drives (FDD)
- Data transfers in DMA or non-DMA mode
- Parallel seek operations on up to four drives
- Compatible with most general-purpose microprocessors
- Single phase 8 MHz clock
- +5V Only
- 40-Pin Dual-In-Line (DIP) package

GENERAL DESCRIPTION

The Z765A is an LSI Floppy Disk Controller (FDC) chip which contains the circuitry and control functions for interfacing a processor to four floppy-disk drives. It supports IBM System 3740 Single Density format (FM) and IBM System 34 Double Density format (MFM) including double-sided recording. The Z765A provides control signals which simplify the design of an external phase locked loop and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a floppy-disk interface. (Figure 1).

Handshaking signals make DMA operation easily incorporated with the aid of an external DMA Controller chip, such as the Z80 DMA. The FDC operates in either the DMA or non-DMA mode. In the non-DMA mode the FDC generates interrupts to the processor every time a data byte is to be transferred. In the DMA mode, the processor need only load the command into the FDC and all data transfers occur under control of the FDC and DMA controllers.

The Z765A executes 15 commands; each command requires multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The commands are:

- READ DATA
- WRITE DATA
- WRITE DELETED DATA
- READ DELETED DATA
- READ TRACK
- READ ID
- FORMAT TRACK
- SCAN EQUAL
- SCAN HIGH OR EQUAL
- SCAN LOW OR EQUAL
- SEEK
- RECALIBRATE
- SENSE INTERRUPT STATUS
- SPECIFY
- SENSE DRIVE STATUS

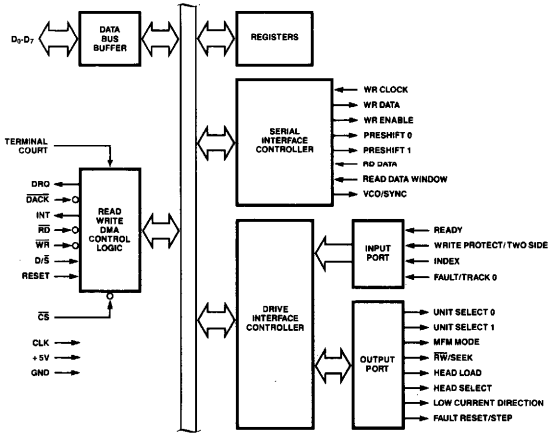


Figure 1. Z765A FDC Block Diagram

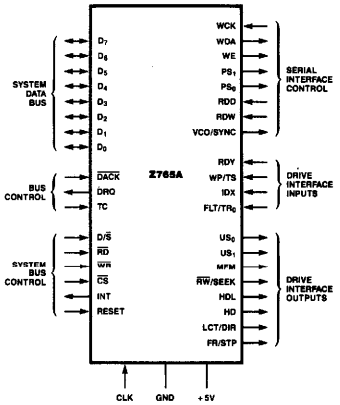


Figure 2. Pin Functions

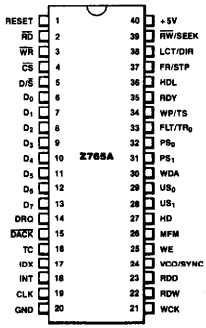


Figure 3. Pin Assignments

2357-001, 002, 003

PIN DESCRIPTIONS (Figures 2 and 3)

CLK. *Clock* (input). Single phase 8MHz square wave clock.

$\overline{CS}$. *Chip Select* (input). IC selected when 0 (Low), allowing $\overline{RD}$ and $\overline{WR}$ to be enabled.

D_0-D_7. *Data Bus.* Bidirectional 8-bit Data Bus. Disabled when $\overline{CS}$ = 1.

$\overline{DACK}$. *DMA Acknowledge* (input). DMA cycle is active when 0, and controller is performing DMA transfer.

DRQ. *Data DMA Request* (output). DMA Request is being made by FDC when DRQ = 1.

D/$\overline{S}$. *Data/Status Register Select* (input). Selects Data Register (D/$\overline{S}$ = 1) or Status Register (D/$\overline{S}$ = 0) contents of the FDC to be sent to Data Bus. Disabled when $\overline{CS}$ = 1.

FR/STP. *Fault Reset/Step* (output). Resets fault FF in FDD in Read/Write mode, contains step pulses to move head to another cylinder in Seek mode.

FLT/TR_0. *Fault/Track 0* (input). Senses FDD fault condition in Read/Write mode and Track 0 condition in Seek mode.

HD. *Head Select* (output). Head 1 selected when 1 (High); Head 0 selected when 0 (Low).

HDL. *Head Load* (output). Command which causes read/write head in FDD to contact diskette.

IDX. *Index* (input). Indicates the beginning of a disk track.

INT. *Interrupt* (output). Interrupt Request generated by FDC.

LCT/DIR. *Low Current/Direction* (output). Lowers Write current on inner tracks in Read/Write mode; determines direction head will step in Seek mode. A fault reset pulse is issued at the beginning of each Read or Write command prior to the occurrence of the Head Load signal.

MFM. *MFM Mode* (output). MFM mode when 1; FM mode when 0.

PS_1, PS_0. *Precompensation (preshift)* (output). Write precompensation status during MFM mode. Determines early, late, and normal times.

$\overline{RD}$. *Read* (input). When 0, control signal for transfer of data from FDC to Data Bus. Disabled when $\overline{CS}$ = 1.

RDD. *Read Data* (input). Read data from FDD, containing clock and data bits.

RDW. *Read Data Window* (input). Generated by PLL, and used to sample data from FDD.

RDY. *Ready* (input). Indicates FDD is ready to send or receive data.

RESET. *Reset* (input). Places FDC in idle state. Resets output lines to FDD to 0. Does not affect SRT, HUT or HLT in Specify command. If RDY pin is held High during Reset, FDC generates an interrupt within 1.024 msec. To clear this interrupt use Sense Interrupt Status command.

$\overline{RW}$/SEEK. *Read Write/Seek* (output). When 1 (High) Seek mode selected; when 0 (Low) Read/Write mode selected.

TC. *Terminal Count* (input). Indicates the termination of a DMA transfer when 1 (High). It terminates data transfer during Read/Write/Scan command in DMA or Interrupt mode.

US_1, US_0. *Unit Select* (output). FDD Unit selected.

VCO/SYNC. (output). Inhibits VCO in PLL when 0 (Low); enables VCO when 1.

WCK. *Write Clock* (input). Write data rate to FDD. FM = 500 KHz, MFM = 1 MHz with a pulse width of 250 ns for both FM and MFM.

WDA. *Write Data* (output). Serial clock and data bits to FDD.

WE. *Write Enable* (output). Enables write data into FDD.

WP/TS. *Write Protect/Two Side* (input). Senses Write Protect status in Read/Write mode and Two-Side Media in Seek mode.

$\overline{WR}$. *Write* (input). When 0, control signal for transfer of data to FDC via Data Bus. Disabled when $\overline{CS}$ = 1.

Table 1. Internal Registers

The bits in the Main Status Register are defined as follows:

Bit No.	Name	Symbol	Description
D_0	FDD 0 Busy	D_0B	FDD number 0 is in the Seek mode. If any bit is set, FDC will not accept read or write command.
D_1	FDD 1 Busy	D_1B	FDD number 1 is in the Seek mode. If any bit is set, FDC will not accept read or write command.
D_2	FDD 2 Busy	D_2B	FDD number 2 is in the Seek mode. If any bit is set, FDC will not accept read or write command.
D_3	FDD 3 Busy	D_3B	FDD number 3 is in the Seek mode. If any bit is set, FDC will not accept read or write command.
D_4	FDC Busy	CB	A read or write command is in process. FDC will not accept any other command.
D_5	Execution Mode	EXM	This bit is set only during execution phase in non-DMA mode. When D_5 goes low, execution phase has ended and result phase has started. It operates only during non-DMA mode of operation.
D_6	Data Input/Output	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO = 1, then transfer is from Data Register to the processor. If DIO = 0, transfer is from the processor to Data Register.
D_7	Request for Master	RQM	Indicates Data Register is ready to send or receive data to or from the processor. Both bits DIO and RQM should be used to perform the handshaking functions of "ready" and "direction" to the processor.

INTERNAL REGISTERS

The Z765A contains two registers which may be accessed by the main system processor: a Status register and a Data register. The 8-bit Main Status register (Table 1) contains the FDC status information and may be accessed at any time. The 8-bit Data register is several registers in a stack; one register at a time is presented to the data bus. The Data register stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data register in order to program or obtain the results after a particular command. Only the Status register may be read and used to facilitate the transfer of data between the processor and Z765A.

The relationship between the Status/Data registers and the signals $\overline{RD}$, $\overline{WR}$, and D/$\overline{S}$ is shown in Table 2.

The Data Input/Output (DIO) and Request for Master (RQM) bits in the Status register indicate when data is ready and the direction transfer on the data bus (Figure 4). The maximum time between the last $\overline{RD}$ or $\overline{WR}$ during a command or result phase and the set or reset DIO and RQM is 12μs; every time the Main Status register is read the CPU should wait 12μs. The maximum time from the trailing edge of the last $\overline{RD}$ in the result phase to when D_4 (FDC busy) goes Low is 12μs.

Table 2. Relationships Between Status/Data Registers and $\overline{RD}$, $\overline{WR}$, and D/$\overline{S}$

D/$\overline{S}$	$\overline{RD}$	$\overline{WR}$	Function
0	0	1	Read Main Status Register
0	1	0	Illegal
0	0	0	Illegal
1	0	0	Illegal
1	0	1	Read from Data Register
1	1	0	Write into Data Register

STATUS REGISTER IDENTIFICATION

Bit No.	Name	Symbol	Description
			Status Register 0
D_7	Interrupt Code	IC	D_7 = 0 and D_6 = 0 Normal Termination of command, (NT). Command was completed and properly executed.
			D_7 = 0 and D_6 = 1 Abnormal Termination of command, (AT). Execution of command was started but was not successfully completed.
D_6			D_7 = 1 and D_6 = 0 Invalid Command issue, (IC). Command which was issued was never started.
			D_7 = 1 and D_6 = 1 Abnormal Termination because during command execution the ready signal from FDD changed state.
D_5	Seek End	SE	When the FDC completes the SEEK command, this flag is set to 1 (High).
D_4	Equipment Check	EC	If a fault signal is received from the FDD, or if the Track 0 signal fails to occur after 77 step pulses (Recalibrate Command) then this flag is set.
D_3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single-sided drive, then this flag is set.
D_2	Head Address	HD	This flag is used to indicate the state of the head at Interrupt.
D_1	Unit Select 1	US_1	This flag is used to indicate a Drive Unit Number at Interrupt.
D_0	Unit Select 0	US_0	This flag is used to indicate a Drive Unit Number at Interrupt.
			Status Register 1
D_7	End of Cylinder	EN	When the FDC tries to access a sector beyond the final sector of a cylinder, this flag is set.
D_6			Not used. This bit is always 0 (Low).
D_5	Data Error	DE	When the FDC detects a Cyclic Redundancy Check (CRC) error in either the ID field or the data field, this flag is set.
D_4	Overrun	OR	If the FDC is not serviced by the host system during data transfers within a certain time interval, this flag is set.
D_3			Not used. This bit always 0 (Low).
D_2	No Data	ND	During execution of READ DATA, WRITE DELETED DATA or SCAN command, if the FDC cannot find the sector specified in the Internal Data Register (IDR), this flag is set.
			During execution of the READ ID command, if the FDC cannot read the ID field without an error, then this flag is set.
			During execution of the READ A cylinder command, if the starting sector cannot be found, then this flag is set.

STATUS REGISTER IDENTIFICATION (Continued)

Bit No.	Name	Symbol	Description
			Status Register 1 (Continued)
D_1	Not Writeable	NW	During execution of WRITE DATA, WRITE DELETED DATA or Format A cylinder command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D_0	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set. If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in data field) of Status register 2 is set.
			Status Register 2
D_7			Not used. This bit is always 0 (Low).
D_6	Control Mark	CM	During execution of the READ DATA or SCAN command, if the FDC encounters a sector which contains a Deleted Data Address Mark, this flag is set.
D_5	Data Error in Data Field	DD	If the FDC detects a CRC error in the data field then this flag is set.
D_4	Wrong Cylinder	WC	This bit is related to the ND bit, and when the contents of Cylinder (C) on the medium is different from that stored in IDR, this flag is set.
D_3	Scan Equal Hit	SH	During execution of the SCAN command, if the condition of "equal" is satisfied, this flag is set.
D_2	Scan Not Satisfied	SN	During execution of the SCAN command, if the FDC cannot find a sector on the cylinder which meets the condition, then this flag is set.
D_1	Bad Cylinder	BC	This bit is related to the ND bit, and when the contents of C on the medium is different from that stored in the IDR and the contents of C is FF_H, then this flag is set.
D_0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.
			Status Register 3
D_7	Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
D_6	Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
D_5	Ready	RY	This bit is used to indicate the status of the Ready signal from the FDD.
D_4	Track 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
D_3	Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD.
D_2	Head Address	HD	This bit is used to indicate the status of the Side Select signal to the FDD.
D_1	Unit Select 1	US_1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D_0	Unit Select 0	US_0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

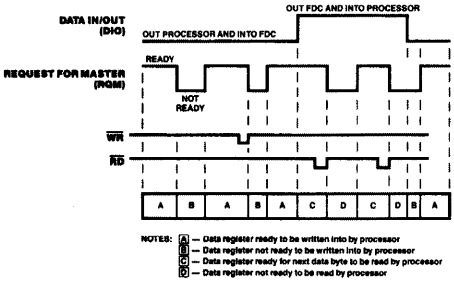


Figure 4. Data Transfer

COMMAND SEQUENCE

The Z765A is capable of performing 15 different commands. Each command is initiated by a multibyte transfer from the processor; the result after execution of the command may also be a multibyte transfer back to the processor. Because of this multibyte interchange of information between the Z765A and the processor, each command consists of three phases:

Command Phase. The FDC receives all information required to perform a particular operation form the processor.

Execution Phase. The FDC performs the operation it was instructed to do.

Result Phase. After completion of the operation, status and other housekeeping information are made available to the processor.

The Instruction set shows the required preset parameters and results for each command. Most commands require 9 command bytes and return 7 bytes during the result phase. The W to the left of each byte indicates a command phase byte to be written; an R indicates a result byte.

PROCESSOR INTERFACE

During Command or Result phases the Main Status register must be read by the processor before each byte of information is written into, or read from, the Data register. Then the CPU should wait for 12μs before reading the Main Status register. Bits D_6 and D_7 in the Main Status register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the Z765A. Many of the commands require multiple bytes and, as a result, the Main Status register must be read prior to each byte transfer to the Z765A. During the Result phase, D_6 and D_7 in the Main Status register must both be 1's before reading each byte from the Data Register. Reading the Main Status register before each byte transfer to the Z765A is required only in the Command and Result phases, not during the Execution phase.

If the Z765A is in the non-DMA mode and reading data from FDD, then the receipt of each data byte is indicated by an interrupt signal on pin 18(INT = 1). The generation of a Read signal ($\overline{RD}$ = 0) or Write signal ($\overline{WR}$ = 0) will clear the interrupt and output the data onto the data bus. If the processor cannot handle interrupts fast enough (every 13μs for the MFM mode and 27μs for the FM mode), then it may poll the Main Status register and bit D_7 (RQM) functions as the interrupt signal. If a Write command is in process, the $\overline{WR}$ signal negates the reset to the interrupt signal.

In the non-DMA mode it is necessary to examine the Main Status register to determine the cause of the interrupt, since it could be a data interrupt or a command termination interrupt, either normal or abnormal. If the Z765A is in the

COMMAND SYMBOL DESCRIPTION

Symbol	Name	Description
D/$\overline{S}$	Data/Status Select	D/$\overline{S}$ controls selection of Main Status register (D/$\overline{S}$ = 0) or Data register (D/$\overline{S}$ = 1)
C	Cylinder Number	C stands for the current/selected cylinder (track) numbers 0 through 76 of the medium.
D	Data	D stands for the data pattern which is going to be written into a sector.
D_7-D_0	Data Bus	8-bit Data Bus, where D_7 stands for a most significant bit, and D_0 stands for a least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the sector.
EOT	End of Track	EOT stands for the final sector number on a cylinder. During Read or Write operations, FDC will stop data transfer after a sector number equal to EOT.
GPL	Gap Length	GPL stands for the length of Gap 3. During Read/Write commands this value determines the number of bytes that VCO/SYNC will stay low after two CRC bytes. During Format command it determines the size of Gap 3.
H	Head Address	H stands for head number 0 or 1, as specified in ID field.
HD	Head	HD stands for a selected head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words.)
HLT	Head Load Time	HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	HUT stands for the head unload time after a Read or Write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	If MF is Low, FM mode is selected, and if it is High. MFM mode is selected.
MT	Multitrack	If MT is high, a Multitrack operation is performed. If MT = 1 after finishing Read/Write operation on side 0, FDC automatically starts searching for sector 1 on side 1.
N	Number	N stands for the Number of data bytes written in a sector.
NCN	New Cylinder Number	NCN stands for a New Cylinder Number or desired position of head which is going to be reached as a result of the Seek operation.
ND	Non-DMA Mode	ND stands for operation in the Non-DMA mode.
PCN	Present Cylinder Number	PCN stands for the cylinder number or present position of Head at the completion of Sense Interrupt Status command.
R	Record	R stands for the sector number which will be read or written.
R/W	Read/Write	R/W stands for either Read (R) or Write (W) signal.
SC	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip	SK stands for Skip Deleted Data Address mark.
SRT	Step Rate Time	SRT stands for the Stepping Rate for the FDD (1 to 16 ms in 1 ms increments). Stepping Rate applies to all drives ($F_{(16)}$ = 1 ms, $E_{(16)}$ = 2 ms, $D_{(16)}$ = 3 ms, . . .).
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	ST0-3 stands for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by D/$\overline{S}$ = 0). ST0-3 may be read only after a command has been executed and contains information relevant to that particular command.
STP	Step	During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); if STP = 2, then alternate sectors are read and compared.
US_0, US_1	Unit Select	Used to select between drives 0-3.

INSTRUCTION SET[1, 2]

Phase	R/W	Data Bus D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Read Data										
Command	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	See Note 3
	W	C								Sector ID information prior to
	W	H								command execution. The 4 bytes
	W	R								are commanded against header
	W	N								on Floppy disk.
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system
Result	R	ST0								Status information after command
	R	ST1								execution
	R	ST2								
	R	C								Sector ID information after
	R	H								command execution
	R	R								
	R	N								
Read Deleted Data										
Command	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	C								Sector ID information prior to
	W	H								command execution. The 4 bytes
	W	R								are commanded against header
	W	N								on Floppy Disk.
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system
Result	R	ST0								Status information after command
	R	ST1								execution
	R	ST2								
	R	C								Sector ID information after
	R	H								command execution
	R	R								
	R	N								

NOTES: 1. Symbols used in this table are described at the end of this section.
2. D/$\overline{S}$ should equal binary 1 for all operations.
3. X = Don't care, usually made to equal binary 0.

INSTRUCTION SET[1, 2] (Continued)

Phase	R/W	Data Bus D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Write Data										
Command	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	C								Sector ID information prior to command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the main system and FDD
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution.
	R	H								
	R	R								
	R	N								
Write Deleted Data										
Command	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	C								Sector ID information prior to command execution. The 4 bytes are commanded against header on Floppy disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

NOTES: 1. Symbols used in this table are described at the end of this section.
2. $D/\overline{S}$ should equal binary 1 for all operations.
3. X = Don't care, usually made to equal binary 0.

INSTRUCTION SET[1, 2] (Continued)

Phase	R/W	Data Bus D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Read A Track										
Command	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	C								Sector ID information prior to command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system. FDC reads all data fields from index hole to EOT.
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								
Read ID										
Command	W	0	MF	0	0	1	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
Execution										The first correct ID information on the cylinder is stored in Data Register.
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information read during Execution phase from Floppy Disk.
	R	H								
	R	R								
	R	N								

NOTES: 1. Symbols used in this table are described at the end of this section.
2. $D/\overline{S}$ should equal binary 1 for all operations.
3. X = Don't care, usually made to equal binary 0.

INSTRUCTION SET[1, 2] (Continued)

Phase	R/W	Data Bus D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Format A Track										
Command	W	0	MF	0	0	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	N								Bytes Sector
	W	SC								Sectors/Track
	W	GPL								Gap 3
	W	D								Filler byte
Execution										FDC formats an entire track.
Result	R	ST0								Status information after command
	R	ST1								execution
	R	ST2								
	R	C								In this case, the ID information
	R	H								has no meaning.
	R	R								
	R	N								
Scan Equal										
Command	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	C								Sector ID information prior to
	W	H								command execution
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data compared between the FDD and the main system.
Result	R	ST0								Status information after command
	R	ST1								execution
	R	ST2								
	R	C								Sector ID information after
	R	H								command execution
	R	R								
	R	N								

NOTES: 1. Symbols used in this table are described at the end of this section.
2. $D/\overline{S}$ should equal binary 1 for all operations.
3. X = Don't care, usually made to equal binary 0.

INSTRUCTION SET[1, 2] (Continued)

Phase	R/W	Data Bus D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Scan Low or Equal										
Command	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	C								Sector ID information prior to
	W	H								command execution
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data compared between the FDD and main system
Result	R	ST0								Status information after command
	R	ST1								execution
	R	ST2								
	R	C								Sector ID information after
	R	H								command execution
	R	R								
	R	N								
Scan High or Equal										
Command	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	C								Sector ID information prior to
	W	H								command execution.
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data compared between the FDD and main system.
Result	R	ST0								Status information after command
	R	ST1								execution
	R	ST2								
	R	C								Sector ID information after
	R	H								command execution.
	R	R								
	R	N								
Recalibrate										
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	X	X	X	X	X	0	US_1	US_0	
Execution										Head retracted to Track 0

NOTES: 1. Symbols used in this table are described at the end of this section.
2. $\overline{DS}$ should equal binary 1 for all operations.
3. X = Don't care, usually made to equal binary 0.

INSTRUCTION SET[1, 2] (Continued)

Phase	R/W	Data Bus D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Sense Interrupt Status										
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	ST0								Status information about the FDC
	R	PCN								at the end of seek operation
Specify										
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	SRT							HUT	
	W	HLT							ND	
Sense Drive Status										
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	X	X	X	X	X	0	US_1	US_0	
Result	R	ST3								Status information about FDD
Seek										
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	NCN								
Execution										Head is positioned over proper cylinder on diskette.
Invalid										
Command	W	Invalid Codes								Invalid Command Codes (NoOp—FDC goes into Standby state.)
Result	R	ST0								ST0 = $80_{(H)}$

NOTES: 1. Symbols used in this table are described at the end of this section.
2. $D/\overline{S}$ should equal binary 1 for all operations.
3. X = Don't care, usually made to equal binary 0.

DMA mode, no interrupts are generated during the Execution phase. The Z765A generates DRQs (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both a $\overline{DACK}$ (DMA Acknowledge) = 0 and an $\overline{RD}$ (Read signal) = 0. When the DMA Acknowledge signal goes Low ($\overline{DACK}$ = 0), then the DMA request is cleared (DRQ = 0). If a Write command has been issued, a $\overline{WR}$ signal appears instead of $\overline{RD}$. After the Execution phase has been completed [Terminal Count (TC) has occurred] or the last sector on the cylinder (EOT) read/written, then an interrupt occurs (INT = 1) which signifies the beginning of the Result phase. When the first byte of data is read during the Result phase, the interrupt is automatically cleared (INT = 0).

The $\overline{RD}$ or $\overline{WR}$ signals should be asserted while $\overline{DACK}$ is true. The $\overline{CS}$ signal is used in conjunction with $\overline{RD}$ and $\overline{WR}$ as a gating function during programmed I/O operations. $\overline{CS}$ has no effect during DMA operations. If the non-DMA mode is chosen, the $\overline{DACK}$ signal should be pulled up to V_{CC}.

During the Result phase all bytes shown in the Command Table must be read. For example, the Read Data command has seven bytes of data in the Result phase; all seven bytes must be read to successfully complete the Read Data command and allow the Z765A to accept a new command.

The Z765A contains five Status registers. The Main Status register can be read at any time by the processor. The other four Status registers (ST0, ST1, ST2, and ST3) are available only during the Result phase and can be read only after completing a command. The particular command that has been executed determines how many of the Status registers are read.

The bytes of data which are sent to the Z765A to form the Command phase and are read out of the Z765A in the Result phase must occur in the order shown in the Command Table. That is, the Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result phases is allowed. After the last byte of data in the Command phase is sent to the Z765A, the Execution phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result phase, the command is automatically ended and the Z765A is ready for a new command.

POLLING FEATURE OF THE Z765A

After Reset is sent to the Z765A, the Unit Select lines US_0 and US_1 automatically go into a polling mode (Figure 5). Between commands (and between step pulses in the Seek command) the Z765A polls all four FDDs looking for a change in the Ready line from any of the drives. If the Ready line changes state (usually due to a door opening or closing), then the Z765A generates an interrupt. When Status register 0 (ST0) is read (after Sense Interrupt Status is issued), Not Ready (NR) is indicated. The polling of the Ready line by the Z765A occurs continuously between commands, thus notifying the processor which drives are on or off line. Each drive is polled every 1.024 ms except during the Read/Write commands. When used with a 4 MHz clock for interfacing to minifloppies, the polling rate is 2.048 ms.

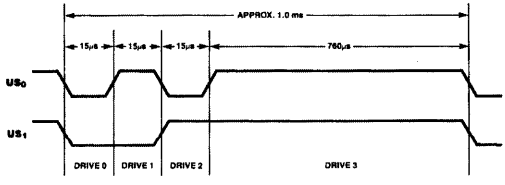


Figure 5. Polling Features

COMMANDS

Read Data

A set of nine (9) byte words are required to place the FDC into the Read Data Mode. After the Read Data command is issued, the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID Address Marks and ID fields. When the current sector number (R) stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC, via the data bus, outputs data byte-to-byte from the data field to the main system.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a Multi-Sector Read Operation. The Read Data command can be terminated by the receipt of a TC signal which should be issued when the DACK for the last byte of data is sent. Upon receipt of this signal, the FDC stops outputting data to the processor, but continues to read data from the current sector, checks Cyclic Redundancy Count (CRC), and at the end of the sector, terminates the Read Data command. The amount of data which can be handled with a single command to the FDC depends upon multitrack (MT), MFM/FM (MF), and Number of Bytes/Sector (N). Table 3 shows the Transfer Capacity.

Table 3. Transfer Capacity

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskettes
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

MT allows the FDC to read data from both sides of the diskette. For a particular cylinder, data is transferred starting at Sector 1, Side 0 and completing at the last sector, Sector L, Side 1. This function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector is not sent to the Data Bus. The FDC internally reads the complete sector performing the CRC check and, depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to FF_H.

At the completion of the Read Data Command the head is unloaded, after the Head Unload Time Interval specified in the Specify Command has elapsed. If the processor issues another command before the head unloads, there is no head settling time between subsequent reads. This time saved is particularly valuable when a diskette is copied.

If the FDC twice detects the index hole without finding the right sector (R), then the FDC sets Status register 1's No Data (ND) flag to 1, and terminates the Read Data command. (Status register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data fields in each sector, the FDC checks the CRC bytes. If a read error is detected indicating incorrect CRC in the ID field, the FDC sets Status register 1's Data Error (DE) flag to 1, and if a CRC error occurs in the Data Field, the FDC also sets Status register 2's Data Error in Data Field (DD) flag to 1, and terminates the Read Data command. (Status register 0, bit 7 = 0, bit 6 = 1.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit D in the first Command Word = 0, then the FDC sets Status register 2's Control Mark (CM) flag to 1, and after reading all the data in the sector, terminates the Read Data command. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector. When SK = 1, the CRC bits in the deleted data field are not checked.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27μs in the FM Mode, and every 13μs in the MFM Mode, or the FDC sets Status register 1's Overrun (OR) flag to 1, and terminates the Read Data command.

If the processor terminates a read or write operation in the FDC, then the ID information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 4 shows the values for C, H, R, and N when the processor terminates the command.

Table 4. C, H, R, and N Values When Processor Terminates Commands

MT	HD	Final Sector Transferred to Processor	ID Information at Result Phase			
			C	H	R	N
0	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	C + 1	NC	R = 01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	C + 1	NC	R = 01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	NC	LSB	R = 01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	C + 1	LSB	R = 01	NC

NOTES: NC (No Change): The same value as the one at the beginning of command execution.
LSB (Least Significant Bit): The least significant bit of H is complemented.

Write Data

A set of nine (9) bytes is required to set the FDC in the Write Data mode. After the Write Data command is issued, the FDC loads the head, waits the specified head setting time, and begins reading ID fields. When all four bytes (C, H, R, and N) loaded during the command match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus and outputs it to the FDD.

After writing data into the current sector, the sector number stored in the R register is incremented by one, and new data is written into the next data field. The FDC continues this Multisector Write Operation until a Terminal Count signal is issued. If a Terminal Count signal is sent to the FDC, it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written, the remainder of the data field is filled with zeros.

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (CRC error) in one of the ID fields, it sets Status register 1's DE flag to 1, and terminates the Write Data command. (Status register 0, bit 7 = 0, bit 6 = 1.)

The Write command operates in the same manner as the Read command for the following items:

- Transfer capacity
- End of cylinder (EN) flag
- No data (ND) flag
- Head unload time interval
- ID information when the processor terminates command
- Definition of DTL when N = 0 and when N ≠ 0

Refer to the Read Data command for details.

In the Write Data mode, data transfers between the processor and FDC via the data bus, must occur every 27μs in the FM mode and every 13μs in the MFM mode. If the time interval between data transfers is longer, then the FDC sets Status register 1's Overrun (OR) flag to 1, and terminates the Write Data command. (Status register 0, bit 7 = 0, bit 6 = 1.)

Write Deleted Data

This command is the same as the Write Data command except a Deleted Data Address mark, instead of the normal Data Address mark, is written at the beginning of the data field.

Read Deleted Data

This command is the same as the Read Data command except that when the FDC detects a Data Address mark at the beginning of a data field and SK = 0, the FDC reads all the data in the sector and sets Status register 2's CM flag to 1, and terminates the command. If SK = 1, then the FDC skips the sector with the Data Address mark and reads the next sector.

Read Track

This command is similar to the Read Data command except that this is a continuous Read operation where the entire data field from each of the sectors is read. Immediately after

sensing the index hole, the FDC starts reading all data fields on the track as continuous blocks of data. If the FDC finds an error in the ID or Data CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR and, if there is no comparison, sets Status register 1's ND flag to 1. Multitrack or skip operations are not allowed with this command.

This command terminates when the number of sectors read is equal to EOT. If the FDC does not find an ID Address mark on the diskette after it senses the index hole for the second time, it sets Status register 1's Missing Address mark (MA) flag to 1 and terminates the command. (Status Register 0, bit 7 = 0, bit 6 = 1.)

Read ID

The Read ID command gives the present position of the recording head. The FDC stores the values from the first ID field it can read. If no proper ID Address mark is found on the diskette before the index hole is encountered for the second time, Status register 1's MA flag is set to 1; if no data is found, Status register 1's No Data (ND) flag is set to 1. The command is then terminated with STO bit 7 = 0 and bit 6 = 1. During this command, data transfer between FDC and the CPU occurs only during the result phase.

Format Track

The Format command allows an entire track to be formatted. After the index hole is detected, data is written on the diskette; Gaps, Address marks, ID fields and data fields, all per the IBM 3740 Single Density format or IBM System 34 Double Density format, are recorded. The processor, during the command phase, supplies values i.e., Number of bytes/sector (N), Sectors Cylinder (SC), Gap Length (GPL), and Data Pattern (D) which determine the particular format to be written.

The data field is filled with the byte of data stored in D. The ID field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for Cylinder number (C), Head number (H), Sector number (R), and Number of bytes/sector (N). This allows diskette formatting with nonsequential sector numbers.

The processor must send new values for C, H, R, and N to the Z765A for each sector on the track. If FDC is set for the DMA mode, it issues four DMA requests per sector. If it is set for the Interrupt mode, it issues four interrupts per sector and the processor must supply C, H, R, and N loads for each sector. The contents of the R register are incremented by 1 after each sector is formatted; thus, the R register contains a value of R when it is read during the Result phase. This incrementing and formatting continues for the whole track until the FDC detects the index hole for the second time, whereupon it terminates the command.

If the Fault signal is received from the FDD at the end of a Write operation, the FDC sets Status register 0's EC flag to 1 and terminates the command after setting Status register 0, bit 7 to 0 and bit 6 to 1. Also the loss of a Ready signal at the beginning of a command execution phase causes Status register 0, bit 7 and 6 to be set to 0 and 1 respectively.

Table 5 shows the sector size relationship between N, SC, and GPL.

Table 5. Functional Description of Commands

Format	Sector Size	N	SC	GPL[1]	GPL[2,3]
8" Standard Floppy					
FM Mode	128 bytes sector	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM Mode[4]	256	01	1A	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
5¼" Minifloppy					
FM Mode	128 bytes/sector	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF
MFM Mode[4]	256	01	12	0A	0C
	256	01	10	20	32
	512	02	08	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF

NOTES:
1. Suggested values of GPL in Read or Write commands to avoid splice point between data field and ID field of contiguous sections.
2. Suggested values of GPL in format command.
3. All values except sector size are hexidecimal.
4. In MFM mode FDC cannot perform a Read/Write format operation with 128 bytes sector (N = 00)

Scan Commands

The Scan commands allow comparison of data read from the diskette and data supplied from the main system. The FDC compares the data on a byte-by-byte basis and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} \leq D_{Processor}$, or $D_{FDD} \geq D_{Processor}$. The hexadecimal byte of FF from memory or from FDD can be used as a mask byte because it always meets the condition of the comparison. One's complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP → R) and the scan operation continues until one of the following conditions occur: the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count (TC) signal is received.

If the conditions for scan are met, the FDC sets the Status register 2's Scan Hit (SH) flag to 1 and terminates the Scan command. If the conditions for scan are not met between the starting sector number (R) and the last sector on the cylinder (EOT), then the FDC sets Status register 2's Scan Not Satisfied (SN) flag to 1, and terminates the Scan command. During the scan operation, the receipt of a signal from the processor or DMA controller causes the FDC to complete the comparison of the particular byte in process and then to terminate the command. Table 6 shows the status of bits SH and SN under various conditions of Scan.

Table 6.

Command	Status Register 2		Comments
	Bit 2 = SN	Bit 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
Scan Low or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} > D_{Processor}$
Scan High or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} > D_{Processor}$
	1	0	$D_{FDD} < D_{Processor}$

If the FDC encounters a Deleted Data Address mark on one of the sectors and SK = 0, then it regards the sector as the last sector on the cylinder, sets Status register 2's Control Mark (CM) flag to 1 and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address mark, reads the next sector, and sets Status register 2's Control Mark (CM) flag to 1 to show that a Deleted sector has been encountered.

When either the Step (STP) (contiguous sectors = 01 or alternate sectors = 02) sectors are read or the Multitrack (MT) is programmed, the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26 and the Scan command is started at sector 21, the following happens. Sectors 21, 23, and 25 are read, then the next sector, 26, is skipped and the index hole is encountered before the EOT value of 26 can be read resulting in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan command would be completed in a normal manner.

During the Scan command, data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having Status register 1's Overrun (OR) flag set, it is necessary to have the data available in less than 27μs (FM mode) or 13μs (MFM mode). If an Overrun occurs, the FDC ends the command with Status register 0, bit 7 cleared to 0 and bit 6 set to 1.

Seek

The Read/Write head within the FDD is moved from cylinder to cylinder under control of the Seek command. The FDC has four independent Present Cylinder registers for each drive which are cleared only after the Recalibrate command. The FDC compares the Present Cylinder Number (PCN) which is the current head position with the New Cylinder Number (NCN), and if there is a difference, performs the following operations:

PCN < NCN: Direction signal to FDD set to 1, and Step Pulses are issued. (Step In)

PCN > NCN: Direction signal to FDD cleared to 0, and Step Pulses are issued. (Step Out)

The rate at which Step pulses are issued is controlled by Stepping Rate Time (SRT) in the Specify command. After each Step pulse is issued NCN is compared against PCN, and when NCN = PCN, Status register 0's Seek End (SE) flag is set to 1, and the command is terminated. At this point FDC interrupt goes High. Bits D_0-D_3 in the Main Status register are set during the Seek operation and are cleared by the Sense Interrupt Status command.

During the command phase of the Seek operation the FDC is in the FDC Busy state, but during the execution phase it is in the Nonbusy state. While the FDC is in the Nonbusy state, another Seek command may be issued, and in this manner parallel Seek operations may be done on up to four drives at once. No other command can be issued for as long as the FDC is in the process of sending step pulses to any drive.

If an FDD is in a Not Ready state at the beginning of the command execution phase or during the Seek operation, then Status register 0's Not Ready (NR) flag is set to 1, and the command is terminated after bit 7 is set to 1 and bit 6 to 0.

If writing three bytes of Seek command exceeds 150μs, the timing between the first two step pulses may be 1ms shorter than that set in the Specify command.

Recalibrate

The function of this command is to retract the Read/Write head within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is Low, the Direction signal remains 0 and step pulses are issued. When the Track 0 signal goes High, the Status register 0's SE flag is set to 1 and the command is terminated. If the Track 0 signal is still Low after 77 step pulses have been issued, the FDC sets Status register 0's SE and Equipment Check (EC) flags to 1s and terminates the command after Status register 0, bit 7 is cleared to 0 and bit 6 is set to 1.

The ability to do overlap Recalibrate commands to multiple FDDs and the loss of the Ready signal, as described in the Seek command, also applies to the Recalibrate command. If the Diskette has more than 77 tracks, the Recalibrate command should be issued twice, in order to position the Read/Write head to Track 0.

Sense Interrupt Status

An interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result phase of command:
   - □ Read Data
   - □ Write Data
   - □ Write Deleted Data
   - □ Read Deleted Data
   - □ Read Track
   - □ Read ID
   - □ Format Track
   - □ Scan
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate command
4. During Execution phase in the non-DMA mode

Interrupts caused by reasons 1 and 4 occur during normal command operations and are easily discernible by the processor. During an execution phase in non-DMA mode, D_5 in the Main Status Register is High. Upon entering the Result phase this bit is cleared. Reasons 1 and 4 do not require Sense Interrupt Status commands. The interrupt is cleared by Reading/Writing data to the FDC. Interrupts caused by reasons 2 and 3 may be uniquely identified with the aid of the Sense Interrupt Status command which resets the Interrupt signal and, via bits 5, 6, and 7 of Status register 0, identifies the cause of the interrupt (Table 7).

Table 7. Interrupt Identification

Seek End	Interrupt Code		
Bit 5	Bit 6	Bit 7	Cause
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate command
1	1	0	Abnormal Termination of Seek or Recalibrate command

The Sense Interrupt Status command is used in conjunction with the Seek and Recalibrate commands which have no result phase. When the disk has reached the desired head position, the Z765A sets the interrupt line true. The host CPU must then issue a Sense Interrupt Status command to determine the actual cause of the interrupt, which could be Seek End or a change in ready status from one of the drives. Figure 6 is a graphic example.

Specify

The Specify command sets the initial values for each of the three internal timers. The Head Unload Time (HUT) defines the time from the end of the execution phase of one of the Read/Write commands to the head unload state. This timer is programmable from 16 to 240ms in increments of 16ms (01 = 16ms, 02 = 32ms...OF_{16} = 240ms). The Step Rate Time (SRT) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16ms in increments of 1ms (F = 1ms, E = 2ms, and D = 3ms). The Head Load Time (HLT) defines the time between the Head Load signal's going High and the start of the Read/Write operation. This timer is programmable from 2 to 254ms in increments of 2ms (01 = 2ms, 02 = 4ms, 03 = 6ms...7F = 254ms).

The time intervals mentioned are a direct function of the 8MHz clock; if the clock were reduced to 4MHz (minifloppy application), all time intervals would be increased by a factor of 2.

The choice of a DMA or non-DMA operation is made by the Non-DMA (ND) bit. When this bit is High (ND = 1), the Non-DMA mode is selected; when ND = 0, the DMA mode is selected.

Sense Drive Status

The processor uses this command to obtain the status of the FDDs. Status register 3 contains the Drive Status information stored internally in FDC registers.

Invalid

If an Invalid command (not defined above) is sent to the FDC, then the FDC terminates the command after Status Register 0 bit 7 is set to 1 and bit 6 to 0. No interrupt is generated by the Z765A during this condition. Bits 6 and 7 (DIO and RQM) in the Main Status register are both High, indicating to the processor that the Z765A is in the Result phase and the contents of Status register 0 (STO) must be read. When the processor reads Status register 0, it finds an 80_H indicating the receipt of an Invalid command.

A Sense Interrupt Status command must be sent after a Seek or Recalibrate Interrupt, otherwise the FDC considers the next command as an Invalid command.

This command may be used as a No-Op command to place the FDC in a standby or No Operation state.

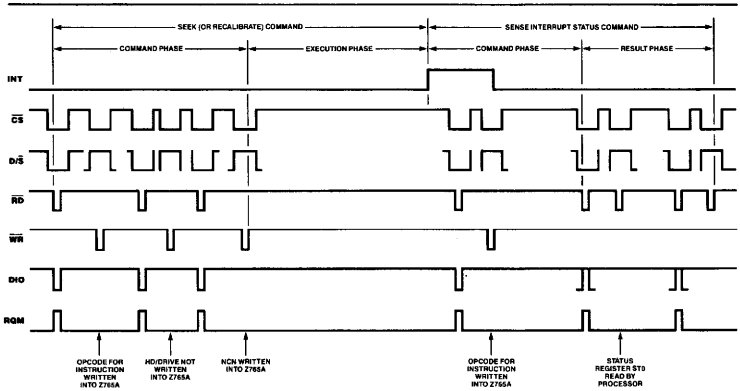


Figure 6. Seek, Recalibrate, and Sense Interrupt Status

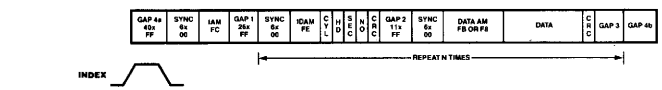


Figure 7. Data Format, FM Mode

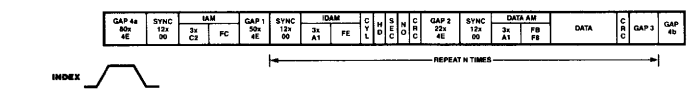


Figure 8. Data Format, MFM Mode

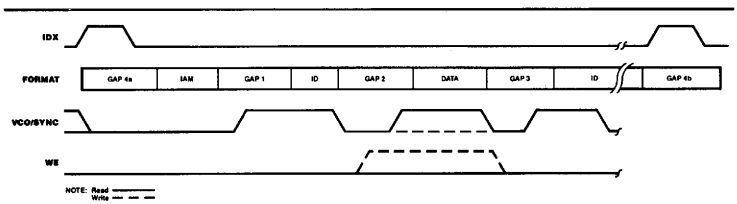


Figure 9. Data Timing Relationships

2357-006, 007, 008, 009

AC CHARACTERISTICS

T_A = −10°C to + 70°C; V_{CC} = +5V ± 5% unless otherwise specified.

Number	Symbol	Parameter	Min	Typ[1]	Max	Unit	Test Condition
			120	125	500	ns	
1	TcC	Clock Cycle Time		125		ns	8" FDD
				250		ns	5¼" FDD
2	TwCh	Clock Width (High)	40			ns	
3	TrC	Clock Rise Time			20	ns	
4	TfC	Clock Fall Time			20	ns	
5	TsAR	D/$\overline{S}$, $\overline{CS}$, $\overline{DACK}$ to $\overline{RD}$ ↓ Setup Time	0			ns	
6	ThRA	D/$\overline{S}$, $\overline{CS}$, $\overline{DACK}$ from $\overline{RD}$ ↑ Hold Time	0			ns	
7	TwRD	$\overline{RD}$ Width	250			ns	
8	TdRDf (Do)	$\overline{RD}$ ↓ to Data Output Delay			200	ns	C_L = 100 pf
9	TdRDr (Dz)	$\overline{RD}$ ↑ to Data Float Delay	20		100	ns	C_L = 100 pf
10	TsCS(WRf)	Control Signal (D/$\overline{S}$, $\overline{CS}$, $\overline{DACK}$) to $\overline{WR}$ ↓ Setup Time	0			ns	
11	ThCS(WRr)	Control Signal (D/$\overline{S}$, $\overline{CS}$, $\overline{DACK}$) from $\overline{WR}$ ↑ Hold Time	0			ns	
12	TwWR	$\overline{WR}$ Width	250			ns	
13	TsD(WRr)	Data to $\overline{WR}$ ↑ Setup Time	150			ns	
14	ThD(WRr)	Data from $\overline{WR}$ ↑ Hold Time	5			ns	
15	TdRDr(INT)	$\overline{RD}$ ↑ to INT Delay Time			500	ns	
16	TdWRr(INT)	$\overline{WR}$ ↑ to INT Delay Time			500	ns	
17	TcDRQ	DRQ Cycle Time	13			µs	
18	TdDRQ(DACK)	$\overline{DACK}$ ↓ to DRQ ↓ Delay			200	ns	
19	TdDACK(DRQ)	DRQ ↑ to $\overline{DACK}$ ↓ Delay	200			ns	TcC = 125 ns
20	TwDACK	$\overline{DACK}$ Width	2			TcC	
21	TwTC	TC Width	1			TcC	
22	TwRST	Reset Width	14			TcC	
				4		µs	MFM = 0 5¼"
23	TcWCK	WCK Cycle Time		2		µs	MFM = 1 5¼"
				2		µs	MFM = 0 8"
				1		µs	MFM = 1 8"
24	TwWCKh	WCK Width (High)	80	250	350	ns	
25	TrWCK	WCK Rise Time			20	ns	
26	TfWCK	WCK Fall Time			20	ns	
27	TdWCKr(PS)	WCK ↑ to Preshift Delay Time	20		100	ns	
28	TdWCKr(WEr)	WCK ↑ to WE ↑ Delay Time	20		100	ns	
29	TdWCKr(WDA)	WCK ↑ to WDA Delay Time	20		100	ns	
30	TwRDDh	RDD Width (High)	40			ns	
				4		µs	MFM = 0 5¼"
31	TWCY	Window Cycle Time		2		µs	MFM = 1 5¼"
				2		µs	MFM = 0 8"
				1		µs	MFM = 1 8"
32	TsW(RDDh) ThW(RDDl)	Window to RDD ↑ Setup Time Window from RDD ↓ Hold Time	15			ns	
33	TsUS(RWh)	Unit Select to $\overline{RW}$/SEEK ↑ Setup Time	12			µs	
34	TsRWr(DIR)	$\overline{RW}$/SEEK ↑ to LCT/DIR Setup Time	7			µs	
35	TsDIR(STEPr)	LCT/DIR to STEP ↑ Setup Time	1			µs	
36	ThUS(STEPl)	Unit Select from STEP ↓ Hold Time	5			µs	

NOTES: 1. Typical values for T_A = 25°C and nominal supply voltage.
2. Under software control, the range is from 1 ms to 16 ms at 8 MHz clock period.

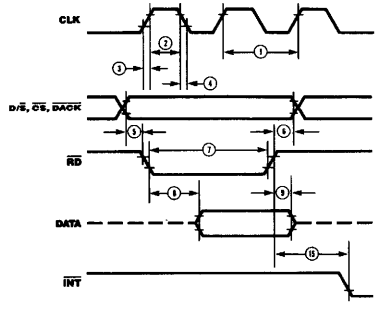
AC CHARACTERISTICS (Continued)

T_A = −10°C to + 70°C; V_{CC} = +5V ± 5% unless otherwise specified.

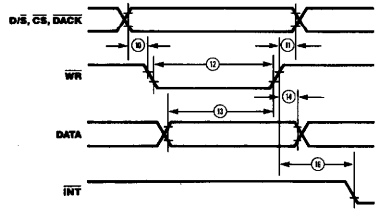
Number	Symbol	Parameter	Min	Typ[1]	Max	Unit	Test Condition
37	TwSTEPh	STEP Width (High)	6	7	8	µs	
38	TcSTEP	STEP Cycle Time	16	Note 2	Note 2	µs	
39	TwFRh	FAULT RESET Width (High)	8		10	µ	
40	TwWDAh	Write Data (WDA) Width (High)	T_D-50			ns	
41	ThUS(SEEKf)	Unit Select from $\overline{RW}$/SEEK ↓ Hold Time	15			µs	
42	ThSEEK(DIR)	$\overline{RW}$/SEEK from LCT/DIR Hold Time	30			µs	
43	ThDIR(STEPf)	LCT/DIR from STEP ↓ Hold Time	24			µs	
44	TwIDX	INDEX Width (High and Low)	10			TcC	
45	TdDRQh(RDI)	DRQ ↑ to $\overline{RD}$ ↓ Delay Time	800			µs	
46	TdDRQh(WRI)	DRQ ↑ to $\overline{WR}$ ↓ Delay Time	250			µs	
47	TdDRQh(RWh)	DRQ ↑ to $\overline{RD}$ ↑ or $\overline{WR}$ ↑ Delay Time			12	µs	

NOTES: 1. Typical values for T_A = 25°C and nominal supply voltage.
2. Under software control, the range is from 1 ms to 16 ms at 8 MHz clock period.

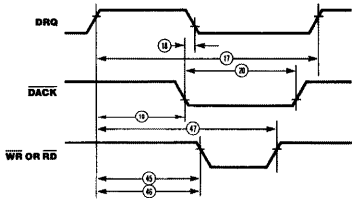
Processor Read Operation



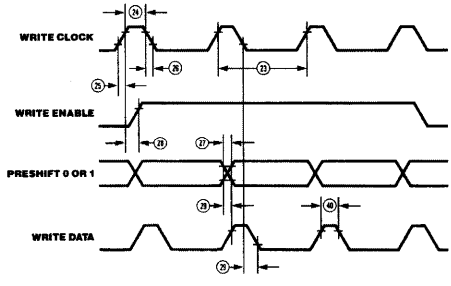
Processor Write Operation



DMA Operation

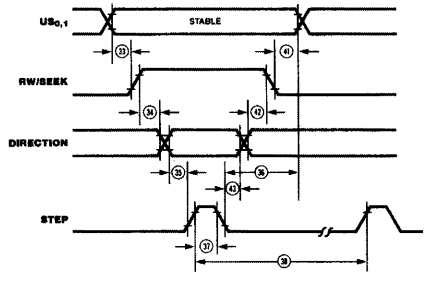


FDD Write Operation



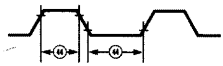
	Preshift 0	Preshift 1
Normal	0	0
Late	0	1
Early	1	0

Seek Operation

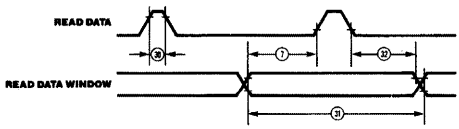


FLT Reset

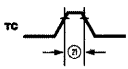
INDEX



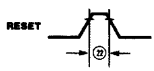
FDD Read Operation



Terminal Count



RESET



ABSOLUTE MAXIMUM RATINGS

T_A = 25°C

Operating Temperature . . . . . .0°C to + 70°C
Storage Temperature . . . . . – 65°C to + 150°C
All Output Voltages . . . . . – .3V to + 7V
All Input Voltages . . . . . – .3V to + 7V
Supply Voltage V_{CC} . . . . . – .3V to + 7V
Power Dissipation 1W

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above these indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_A = 0°C to + 70°C; V_{CC} = + 5V ± 5% unless otherwise specified.

Symbol	Parameter	Min	Typ*	Max	Unit	Test Condition
V_{IL}	Input Low Voltage	– 0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.40	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OH} = – 200 μA
V_{ILC}	Input Low Voltage (CLK + WR Clock)	– 0.3		0.45	V	
V_{IHC}	Input High Voltage (CLK + WR Clock)	2.4		V_{CC} + 0.3	V	
I_{CC}	V_{CC} Supply Current			150	mA	
I_{LI}	Input Load Current (All Input Pins)			10	μA	V_{IN} = V_{CC}
				– 10	μA	V_{IN} = 0V
I_{LOH}	High Level Output Leakage Current			10	μA	V_{OUT} = V_{CC}
I_{LOL}	Low Level Output Leakage Current			– 10	μA	V_{OUT} = + 0.40V

*Typical values for T_A = 25°C and nominal supply voltage.

CAPACITANCE

T_A = 25°C; f_c = 1 MHz; V_{CC} = 0V

Symbol	Parameter	Min	Max	Unit	Test Condition
C_{CLOCK}	Clock Input Capacitance		20	pF	All pins except pin under
C_{IN}	Input Capacitance		10	pF	test tied to AC Ground
C_{OUT}	Output Capacitance		20	pF	

ORDERING INFORMATION

Ordering information is available from your local Zilog Sales Office.

Package drawings are in the Package Information section in this book.

Refer to the Literature List for additional documentation.

00-2357-01

National Semiconductor

Preliminary
May 1980

INS8250-B Asynchronous Communications Element

General Description

The INS8250 is a programmable Asynchronous Communications Element (ACE) chip contained in a standard 40-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate technology, functions as a serial data input/output interface in a microcomputer system. The functional configuration of the INS8250 is programmed by the system software via a TRI-STATE® 8-bit bidirectional data bus.

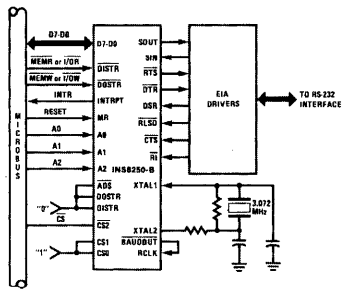
The INS8250 performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the INS8250 at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the INS8250, as well as any error conditions (parity, overrun, framing, or break interrupt).

In addition to providing control of asynchronous data communications, the INS8250 includes a programmable Baud Generator that is capable of dividing the timing reference clock input by divisors of 1 to $(2^{16} - 1)$, and producing a 16x clock for driving the internal transmitter logic. Provisions are also included to use this 16x clock to drive the receiver logic. Also included in the INS8250 is a complete MODEM-control capability, and a processor-interrupt system that may be software tailored to the user's requirements to minimize the computing time required to handle the communications link.

Features

- Designed to be Easily Interfaced to Most Popular Microprocessors.
- Adds or Deletes Standard Asynchronous Communication Bits (Start, Stop, and Parity) to or from Serial Data Stream
- Full Double Buffering Eliminates Need for Precise Synchronization
- Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts
- Programmable Baud Rate Generator Allows Division of Any Input Clock by 1 to $(2^{16} - 1)$ and Generates the Internal 16x Clock
- Independent Receiver Clock Input
- MODEM Control Functions (CTS, RTS, DSR, DTR, RI, and Carrier Detect)
- Fully Programmable Serial-Interface Characteristics
  - 5-, 6-, 7-, or 8-Bit Characters
  - Even, Odd, or No-Parity Bit Generation and Detection
  - 1-, 1½-, or 2-Stop Bit Generation
  - Baud Rate Generation (DC to 56k Baud)
- False Start Bit Detection
- Complete Status Reporting Capabilities
- TRI-STATE TTL Drive Capabilities for Bidirectional Data Bus and Control Bus
- Line Break Generation and Detection
- Internal Diagnostic Capabilities
  - Loopback Controls for Communications Link Fault Isolation
  - Break, Parity, Overrun, Framing Error Simulation
- Full Prioritized Interrupt System Controls
- Single +5-Volt Power Supply
- MICROBUS™* Compatible

INS8250-B MICROBUS Configuration



*Trademark, National Semiconductor Corp.

μPG-FL5M50/Printed in U.S.A.

Absolute Maximum Ratings

Temperature Under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
All Input or Output Voltages with Respect to V_{SS} . . . . −0.5 V to +7.0 V
Power Dissipation . . . . . 400 mW

Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.

DC Electrical Characteristics

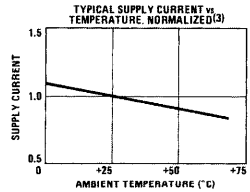
T_A = 0°C to +70°C, V_{CC} = +5 V ± 5%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{ILX}	Clock Input Low Voltage	−0.5		0.8	V	
V_{IHX}	Clock Input High Voltage	2.0		V_{CC}	V	
V_{IL}	Input Low Voltage	−0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 1.6 mA on all outputs,
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −100 μA
I_{CC} (AV)	Avg Power Supply Current (V_{CC})		65	80	mA	
I_{IL}	Input Leakage			±10	μA	
I_{CL}	Clock Leakage			±10	μA	

Capacitance

T_A = 25°C, V_{CC} = V_{SS} = 0 V

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
C_{XIN}	Clock Input Capacitance		15	20	pF	
C_{XOUT}	Clock Output Capacitance		20	30	pF	f_c = 1 MHz
C_{IN}	Input Capacitance		6	10	pF	Unmeasured pins returned to V_{SS}
C_{OUT}	Output Capacitance		10	20	pF	



AC Electrical Characteristics

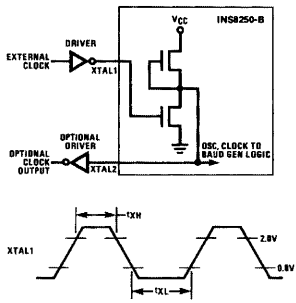
T_A = 0°C to ± 70°C, V_{CC} ± 5%

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{AW}	Address Strobe Width	120	—	ns	
t_{AS}	Address Setup Time	110	—	ns	
t_{AH}	Address Hold Time	60	—	ns	
t_{CS}	Chip Select Setup Time	110	—	ns	
t_{CH}	Chip Select Hold Time	60	—	ns	
t_{CSS}	Chip Select Output Delay from Strobe	0	100	ns	-@ 100pF loading
t_{DID}	$\overline{\text{DISTR}}$/DISTR Strobe Delay	0	—	ns	
t_{DIW}	$\overline{\text{DISTR}}$/DISTR Strobe Width	350	—	ns	
t_{RC}	Read Cycle Delay	1735	—	ns	
RC	Read Cycle = t_{AW} + t_{DID} + t_{DIW} + t_{RC}	2205	—	ns	
t_{DD}	$\overline{\text{DISTR}}$/DISTR to Driver Disable Delay	—	250	ns	-@ 100 pF loading
t_{DDD}	Delay from DISTR/$\overline{\text{DISTR}}$ to Data	—	300	ns	-@ 100 pF loading
t_{HZ}	$\overline{\text{DISTR}}$/DISTR to Floating Data Delay	100	—	ns	-@ 100 pF loading
t_{DOD}	$\overline{\text{DOSTR}}$/DOSTR Strobe Delay	50	—	ns	
t_{DOW}	$\overline{\text{DOSTR}}$/DOSTR Strobe Width	350	—	ns	
t_{WC}	Write Cycle Delay	1785	—	ns	
WC	Write Cycle = t_{AW} + t_{DOD} + t_{DOW} + t_{WC}	2305	—	ns	
t_{DS}	Data Setup Time	350	—	ns	
t_{DH}	Data Hold Time	100	—	ns	
t_{CSC}*	Chip Select Output Delay from Select	—	200	ns	-@ 100pF loading
t_{RA}*	Address Hold Time from $\overline{\text{DISTR}}$/DISTR	50	—	ns	
t_{RCS}*	Chip Select Hold Time from $\overline{\text{DISTR}}$/DISTR	50	—	ns	
t_{AR}*	$\overline{\text{DISTR}}$/DISTR Delay from Address	110	—	ns	
t_{CSR}*	$\overline{\text{DISTR}}$/DISTR Delay from Chip Select	110	—	ns	
t_{WA}*	Address Hold Time from $\overline{\text{DOSTR}}$/DOSTR	50	—	ns	
t_{WCS}*	Chip Select Hold Time from $\overline{\text{DOSTR}}$/DOSTR	50	—	ns	
t_{AW}*	$\overline{\text{DOSTR}}$/DOSTR Delay from Address	160	—	ns	
t_{CSW}*	$\overline{\text{DOSTR}}$/DOSTR Delay from Select	160	—	ns	
t_{MRW}	Master Reset Pulse Width	25	—	μs	

*Applicable only when ADS input is tied permanently low.

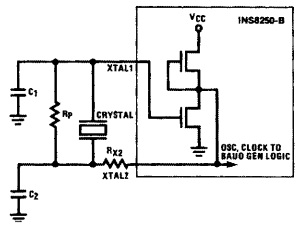
AC Electrical Characteristics (cont'd.)

Symbol	Parameter	Min	Max	Units	Test Conditions
BAUD GENERATOR					
N	Baud Rate Divisor	1	$2^{16}-1$		
t_{BLD}	Baud Output Negative Edge Delay		250 typ	ns	100 pF Load
t_{BHD}	Baud Output Positive Edge Delay		250 typ	ns	100 pF Load
t_{LW}	Baud Output Down Time	425 typ		ns	100 pF Load
t_{HW}	Baud Output Up Time	330 typ		ns	100 pF Load
RECEIVER					
t_{SCD}	Delay from RCLK to Sample Time		2 typ	μs	
t_{SINT}	Delay from Stop to Set Interrupt		2 typ	μs	100 pF Load
t_{RINT}	Delay from $\overline{DISTR}$/DISTR (RD RBR/RDLSR) to Reset Interrupt		1 typ	μs	100 pF Load
TRANSMITTER					
t_{HR}	Delay from $\overline{DOSTR}$/DOSTR (WR THR) to Reset Interrupt		1 typ	μs	100 pF Load
t_{IRS}	Delay from Initial INTR Reset to Transmit Start		16 typ	$\overline{BAUDOUT}$ Cycles	
t_{SI}	Delay from Initial Write to Interrupt		24 typ	$\overline{BAUDOUT}$ Cycles	
t_{SS}	Delay from Stop to Next Start		1 typ	μs	
t_{STI}	Delay from Stop to Interrupt (THRE)		8 typ	$\overline{BAUDOUT}$ Cycles	
t_{IR}	Delay from $\overline{DISTR}$/DISTR (RD IIR) to Reset Interrupt (THRE)		1 typ	μs	100 pF Load
MODEM CONTROL					
t_{MDO}	Delay from DOSTR/$\overline{DOSTR}$ (WR MCR) to Output		1 typ	μs	100 pF Load
t_{SIM}	Delay to Set Interrupt from MODEM Input		1 typ	μs	100 pF Load
t_{RIM}	Delay to Reset Interrupt from $\overline{DISTR}$/DISTR (RD MSR)		1 typ	μs	100 pF Load



Timing	Min	Units
t_{XH}	140	ns
t_{XL}	140	ns

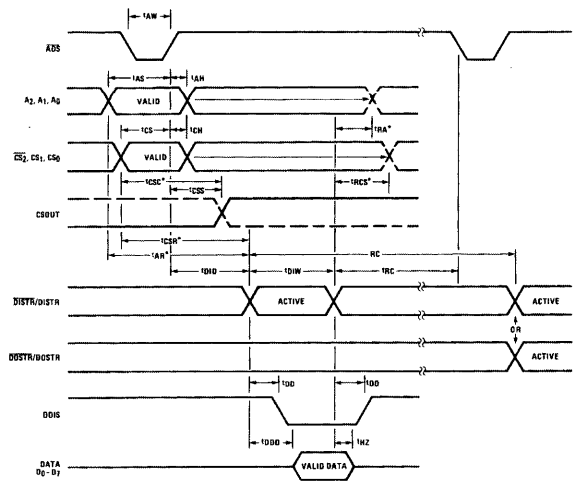
A. External Clock Input (3.1 MHz Max.)



CRYSTAL	R_P	R_{X2}	C_1	C_2
3.1 MHz	1 MΩ	1.5K	10 - 30 pF	40 - 60 pF

B. Typical Crystal Oscillator Network

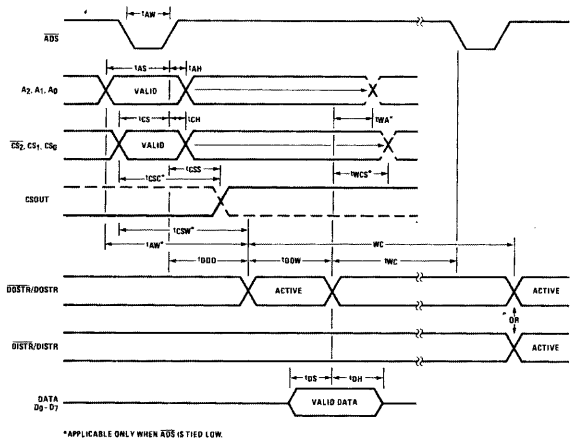
Timing Waveforms



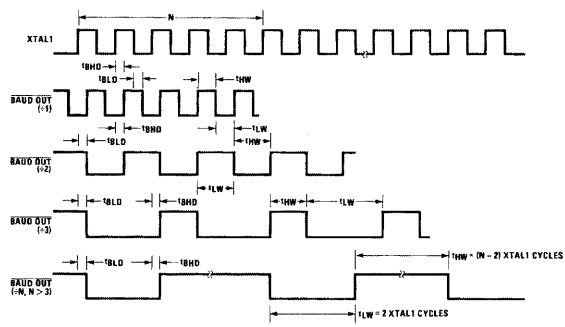
*APPLICABLE ONLY WHEN ADS IS TIED LOW.

Read Cycle

Timing Waveforms (cont'd.)

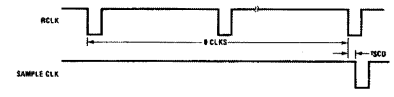


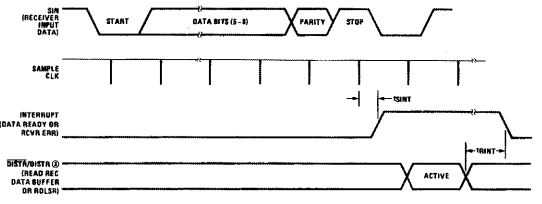
Write Cycle



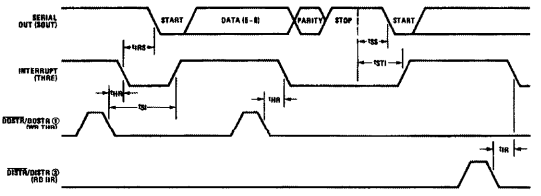
BAUDOUT Timing

Timing Waveforms (cont'd.)

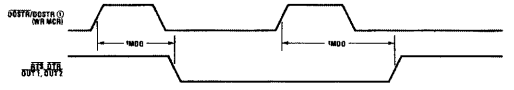


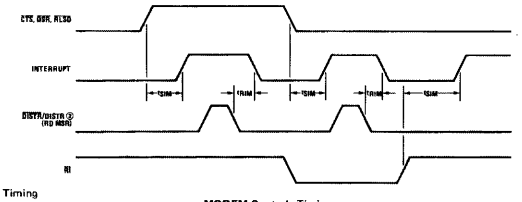


Receiver Timing



Transmitter Timing

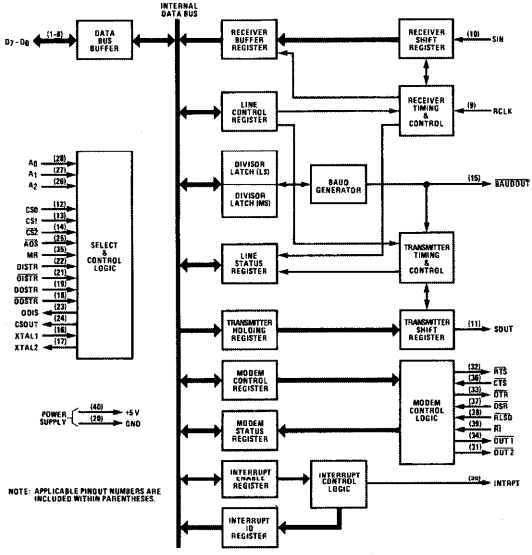




MODEM Controls Timing

NOTES:
① See Write Cycle Timing
② See Read Cycle Timing

INS8250-B Block Diagram



INS8250-B Functional Pin Description

The following describes the function of all INS8250 input/output pins. Some of these descriptions reference internal circuits.

NOTE

In the following descriptions, a low represents a logic 0 (0 volt nominal) and a high represents a logic 1 (+2.4 volts nominal).

INPUT SIGNALS

Chip Select (CS0, CS1, $\overline{CS2}$), Pins 12 – 14: When CS0 and CS1 are high and $\overline{CS2}$ is low, the chip is selected. Chip selection is complete when the decoded chip select signal is latched with an active (low) Address Strobe ($\overline{ADS}$) input. This enables communication between the INS8250 and the CPU.

Data Input Strobe (DISTR, $\overline{DISTR}$), Pins 22 and 21: When DISTR is high or $\overline{DISTR}$ is low while the chip is selected, allows the CPU to read status information or data from a selected register of the INS8250.

NOTE

Only an active DISTR or $\overline{DISTR}$ input is required to transfer data from the INS8250 during a read operation. Therefore, tie either the DISTR input permanently low or the $\overline{DISTR}$ input permanently high, if not used.

Data Output Strobe (DOSTR, $\overline{DOSTR}$), Pins 19 and 18: When DOSTR is high or $\overline{DOSTR}$ is low while the chip is selected, allows the CPU to write data or control words into a selected register of the INS8250.

NOTE

Only an active DOSTR or $\overline{DOSTR}$ input is required to transfer data to the INS8250 during a write operation. Therefore, tie either the DOSTR input permanently low or the $\overline{DOSTR}$ input permanently high, if not used.

Address Strobe ($\overline{ADS}$), Pin 25: When low, provides latching for the Register Select (A0, A1, A2) and Chip Select (CS0, CS1, $\overline{CS2}$) signals.

NOTE

An active $\overline{ADS}$ input is required when the Register Select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, tie the $\overline{ADS}$ input permanently low.

Register Select (A0, A1, A2), Pins 26 – 28: These three inputs are used during a read or write operation to select an INS8250 register to read from or write into as indicated in the table below. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain INS8250 registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches.

DLAB	A_2	A_1	A_0	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	None
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

Master Reset (MR), Pin 35: When high, clears all the registers (except the Receiver Buffer, Transmitter Holding, and Divisor Latches), and the control logic of the INS8250. Also, the state of various output signals (SOUT, INTRPT, $\overline{OUT1}$, $\overline{OUT2}$, $\overline{RTS}$, $\overline{DTR}$) are affected by an active MR input. (Refer to table 1.)

Receiver Clock (RCLK), Pin 9: This input is the 16x baud rate clock for the receiver section of the chip.

Serial Input (SIN), Pin 10: Serial data input from the communications link (peripheral device, MODEM, or data set).

Clear to Send ($\overline{CTS}$), Pin 36: The $\overline{CTS}$ signal is a MODEM control function input whose condition can be tested by the CPU by reading bit 4 (CTS) of the MODEM Status Register. Bit 0 (ΔCTS) of the MODEM Status Register indicates whether the $\overline{CTS}$ input has changed state since the previous reading of the MODEM Status Register.

NOTE

Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Data Set Ready ($\overline{DSR}$), Pin 37: When low, indicates that the MODEM or data set is ready to establish the communications link and transfer data with the INS8250. The $\overline{DSR}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 5 (DSR) of the MODEM Status Register. Bit 1 (DDSR) of the MODEM Status Register indicates whether the $\overline{DSR}$ input has changed state since the previous reading of the MODEM Status Register.

NOTE

Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Received Line Signal Detect ($\overline{RLSD}$), Pin 38: When low, indicates that the data carrier has been detected by the MODEM or data set. The $\overline{RLSD}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 7 (RLSD) of the MODEM Status Register. Bit 3 (DRLSD) of the MODEM Status Register indicates whether the $\overline{RLSD}$ input has changed state since the previous reading of the MODEM Status Register.

NOTE

Whenever the RLSD bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Ring Indicator ($\overline{RI}$), Pin 39: When low, indicates that a telephone ringing signal has been received by the MODEM or data set. The $\overline{RI}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 6 (RI) of the MODEM Status Register. Bit 2 (TERI) of the MODEM Status Register indicates whether the $\overline{RI}$ input has changed from a low to a high state since the previous reading of the MODEM Status Register.

NOTE

Whenever the RI bit of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM Status Interrupt is enabled.

V_{CC}, Pin 40: +5-volt supply.

V_{SS}, Pin 20: Ground (0-volt) reference.

OUTPUT SIGNALS

Data Terminal Ready ($\overline{DTR}$), Pin 33: When low, informs the MODEM or data set that the INS8250 is ready to communicate. The DTR output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. The $\overline{DTR}$ signal is set high upon a Master Reset operation.

Request to Send ($\overline{RTS}$), Pin 32: When low, informs the MODEM or data set that the INS8250 is ready to transmit data. The $\overline{RTS}$ output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register. The $\overline{RTS}$ signal is set high upon a Master Reset operation.

Output 1 ($\overline{OUT1}$), Pin 34: User-designated output that can be set to an active low by programming bit 2 ($\overline{OUT1}$) of the MODEM Control Register to a high level. The $\overline{OUT1}$ signal is set high upon a Master Reset operation.

Output 2 ($\overline{OUT2}$), Pin 31: User-designated output that can be set to an active low by programming bit 3 ($\overline{OUT2}$) of the MODEM Control Register to a high level. The $\overline{OUT2}$ signal is set high upon a Master Reset operation.

Chip Select Out (CSOUT), Pin 24: When high, indicates that the chip has been selected by active CS0, CS1, and $\overline{CS2}$ inputs. No data transfer can be initiated until the CSOUT signal is a logic 1.

Driver Disable (DDIS), Pin 23: Goes low whenever the CPU is reading data from the INS8250. A high-level DDIS output can be used to disable an external transceiver (if used between the CPU and INS8250 on the D_7 - D_0 Data Bus) at all times, except when the CPU is reading data.

Baud Out ($\overline{BAUDOUT}$), Pin 15: 16x clock signal for the transmitter section of the INS8250. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. The $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to the RCLK input of the chip.

Interrupt (INTRPT), Pin 30: Goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Error Flag; Received Data Available; Transmitter Holding Register Empty; and MODEM Status. The INTRPT signal is reset low upon the appropriate interrupt service or a Master Reset operation.

Serial Output (SOUT), Pin 11: Composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Marking (logic 1) state upon a Master Reset operation.

INPUT/OUTPUT SIGNALS

Data (D_7 - D_0) Bus, Pins 1 - 8: This bus comprises eight TRI-STATE input/output lines. The bus provides bidirectional communications between the INS8250 and the CPU. Data, control words, and status information are transferred via the D_7 - D_0 Data Bus.

External Clock Input/Output (XTAL 1, XTAL 2), Pins 16 and 17: These two pins connect the main timing reference (crystal or signal clock) to the INS8250.

Pin Configuration

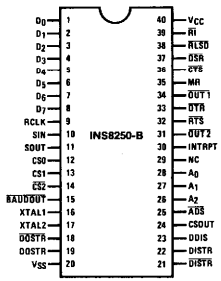


Table 1. ACE Reset Functions

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	All Bits Low (0 - 3 forced and 4 - 7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1 and 2 Low Bits 3 - 7 are Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, Except Bits 5 & 6 are High
MODEM Status Register	Master Reset	Bits 0 - 3 Low Bits 4 - 7 — Input Signal
SOUT	Master Reset	High
INTRPT (RCVR Errs)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read RBR/MR	Low
INTRPT (THRE)	Read IIR/Write THR/MR	Low
INTRPT (Modem Status Changes)	Read MSR/MR	Low
$\overline{OUT\ 2}$	Master Reset	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
$\overline{OUT\ 1}$	Master Reset	High

INS8250-B Accessible Registers

The system programmer may access or control any of the INS8250 registers summarized in table 2 via the CPU. These registers are used to control INS8250 operations and to transmit and receive data.

INS8250 LINE CONTROL REGISTER

The system programmer specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the programmer may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The contents of the Line Control Register are indicated in table 2 and are described below.

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits in each transmitted or received serial character. If bit 2 is a logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, 1½ Stop bits are generated or checked. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 Stop bits are generated or checked.

Table 2. Summary of INS8250-B Accessible Registers

	Register Address									
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	3	4	5	6	0 DLAB = 1	1 DLAB = 1
Bit No.	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Identification Register (Read Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Divisor Latch (LS)	Divisor Latch (MS)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	DLL	DLM
0	Data Bit 0*	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OR)	Delta Data Set Ready (DDSR)	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Receive Line Signal Detect (DRLSD)	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Shift Register Empty (TSRE)	Ring Indicator (RI)	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Received Line Signal Detect (RLSD)	Bit 7	Bit 15

* Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and then detected by the receiver as a logic 0 if bit 4 is a logic 1 or as a logic 1 if bit 4 is a logic 0.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state and remains there regardless of other transmitter activity. The set break is disabled by setting bit 6 to a logic 0. This feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

INS8250 PROGRAMMABLE BAUD RATE GENERATOR

The INS8250 contains a programmable Baud Rate Generator that is capable of taking any clock input (DC to 3.1 MHz) and dividing it by any divisor from 1 to $(2^{16}-1)$. The output frequency of the Baud Generator is 16x the Baud rate [divisor # = (frequency input) ÷ (baud rate x 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 3 and 4 illustrate the use of the Baud Rate Generator with crystal frequencies of 1.8432 MHz and 3.072 MHz respectively. For baud rates of 38400 and below the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen.

NOTE

The maximum operating frequency of the Baud Generator is 3.1 MHz. However, when using divisors of 3 and below, the maximum frequency is equal to the divisor in MHz. For example, if the divisor is 1, then the maximum frequency is 1 MHz. In no case should the data rate be greater than 56k Baud.

LINE STATUS REGISTER

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated in table 2 and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 may be reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register or by writing a logic 0 into it from the CPU.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Table 3. Baud Rates Using 1.8432 MHz Crystal

Desired Baud Rate	Divisor Used to Generate 16x Clock	Percent Error Difference Between Desired & Actual
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.69
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.86

NOTE: 1.8432 MHz is the standard 8080 frequency divided by 10.

Table 4. Baud Rates Using 3.072 MHz Crystal

Desired Baud Rate	Divisor Used to Generate 16x Clock	Percent Error Difference Between Desired & Actual
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.23
9600	20	–
19200	10	–
38400	5	–

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level).

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits).

NOTE

Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the INS8250 is ready to accept a new character for transmission. In addition, this bit causes the INS8250 to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Shift Register Empty (TSRE) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Shift Register is idle. It is reset to logic 0 upon a data transfer from the Transmitter Holding Register to the Transmitter Shift Register. Bit 6 is a read-only bit.

Bit 7: This bit is permanently set to logic 0.

INTERRUPT IDENTIFICATION REGISTER

The INS8250 has an on-chip interrupt capability that allows for complete flexibility in interfacing to all the popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the INS8250 prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and the type of that interrupt are stored in the Interrupt Identification Register (refer to table 5). The Interrupt Identification Register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in table 2 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in table 5.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Table 5. Interrupt Control Functions

Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	1	–	None	None	–
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

INTERRUPT ENABLE REGISTER

This 8-bit register enables the four types of interrupts of the INS8250 to separately active the chip Interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are indicated in table 2 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

MODEM CONTROL REGISTER

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in table 2 and are described below.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

NOTE

The $\overline{DTR}$ output of the INS8250 may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 ($\overline{OUT\,1}$) signal, which is an auxiliary user-designated output. Bit 2 affects the $\overline{OUT\,1}$ output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 ($\overline{OUT\,2}$) signal, which is an auxiliary user-designated output. Bit 3 affects the $\overline{OUT\,2}$ output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a loopback feature for diagnostic testing of the INS8250. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$, and $\overline{RI}$) are disconnected; and the four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT\,1}$, and $\overline{OUT\,2}$) are internally connected to the four MODEM Control inputs. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the INS8250.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

The INS8250 interrupt system can be tested by writing into the lower six bits of the Line Status Register and the lower four bits of the MODEM Status Register. Setting any of these bits to a logic 1 generates the appropriate interrupt (if enabled). The resetting of these interrupts is the same as in normal INS8250 operation. To return to normal operation, the registers must be reprogrammed for normal operation and then bit 4 of the MODEM Control Register must be reset to logic 0.

Bits 5 through 7: These bits are permanently set to logic 0.

MODEM STATUS REGISTER

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in table 2 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the $\overline{RLSD}$ input to the chip has changed state.

NOTE

Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR.

Bit 7: This bit is the complement of the Received Line Signal Detect ($\overline{RLSD}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 2 of the MCR.

Typical Applications

Figures 1 and 2 show how to use the INS8250 chip in an INS8080A system and in a microcomputer system with a high-capacity data bus.

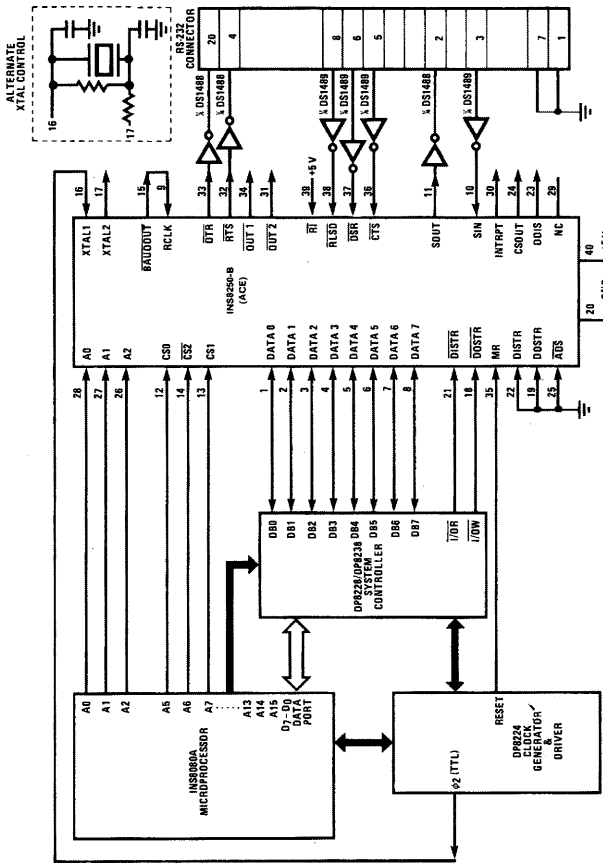


Figure 1. Typical INS8080A/INS8250-B RS-232 Terminal Interface

Typical Applications (cont'd)

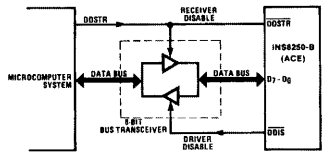
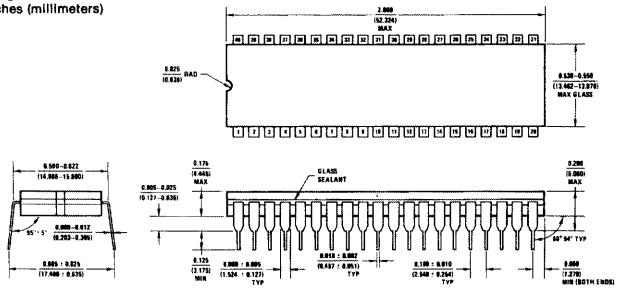


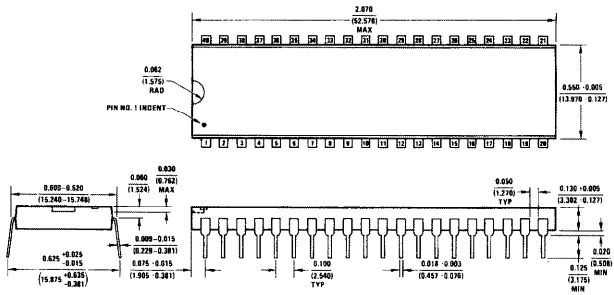
Figure 2. Typical Interface for a High-Capacity Data Bus

Physical Dimensions

inches (millimeters)



Ceramic Dual-In-Line Package [Cerdip (J)]
Order Number INS8250J-B



Plastic Dual-In-Line Package (N)
Order Number INS8250N-B

National Semiconductor Corporation
2900 Semiconductor Drive
Santa Clara, CA. 95051
Tel: (408)737-5000
TWX: (910)339-9240

National Semiconductor GmbH
Eisenheimerstrasse 61/111
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West Germany
Tel: (089)576091
Telex: 05-22772

NS International Inc., Japan
Miyake Building
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Tokyo, Japan
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TWX: 232-2015 NSCJ—J

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Kowloon, Hong Kong
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Cable: NATSEMI

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Australia
Tel: 03-729-6333
Telex: 32096

OKI semiconductor

MSM6242RS/GS

DIRECT BUS CONNECTED CMOS REAL TIME CLOCK/CALENDAR

GENERAL DESCRIPTION

The MSM6242 is a silicon gate CMOS Real Time Clock/Calendar for use in direct bus-connection Microprocessor/Microcomputer applications. An on-chip 32.768KHz crystal oscillator time base is divided to provide addressable 4-bit I/O data for SECONDS, MINUTES, HOURS, DAY OF WEEK, DATE, MONTH and YEAR. Data access is controlled by 4-bit address, chip selects ($\overline{CS0}$, CS1), $\overline{WRITE}$, $\overline{READ}$, and ALE. Control Registers D, E and F provide for 30 SECOND error adjustment, INTERRUPT REQUEST (IRQ FLAG) and BUSY status bits, clock STOP, HOLD, and RESET FLAG bits, 4 selectable INTERRUPTS rates are available at the STD.P (STANDARD PULSE) output utilizing Control Register inputs T0, T1 and the ITRPT/STND (INTERRUPT/STANDARD). Masking of the interrupt output (STD.P) can be accomplished via the MASK bit. The MSM6242 can operate in a 12/24 hour format and Leap Year timing is automatic.

The MSM6242 normally operates from a 5V ± 10% supply at −30 to 85°C. Battery backup operation down to 2.0V allows continuation of time keeping when main power is off. The MSM6242 is offered in a 18-pin plastic DIP and FLAT package.

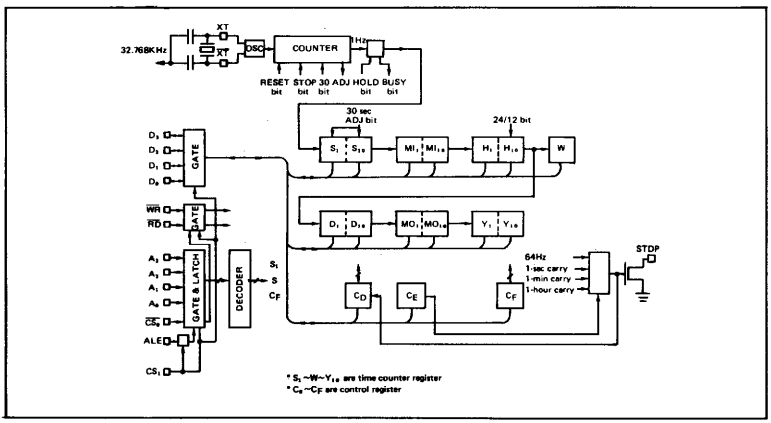
FEATURES

DIRECT MICROPROCESSOR/MICROCONTROLLER BUS CONNECTION

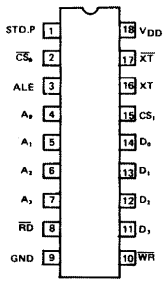
TIME	MONTH	DATE	YEAR	DAY OF WEEK
23:59:59	12	31	80	7

- 4-bit data bus
- 4-bit address bus
- $\overline{READ}$, $\overline{WRITE}$, ALE and CHIP SELECT INPUTS
- Status registers — IRQ and BUSY
- Selectable interrupt outputs — 1/64 second, 1 second, 1 minute, 1 hour
- Interrupt masking
- 32.768KHz crystal controlled operation
- 12/24 hour format
- Auto leap year
- ±30 second error correction
- Single 5V supply
- Battery backup down to V_{DD} = 2.0V
- Low power dissipation:
  20 μW max at V_{DD} = 2V
  150 μW max at V_{DD} = 5V
- 18-pin plastic DIP package

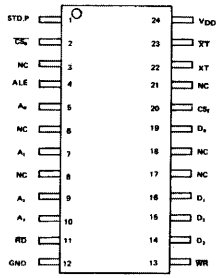
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



18 pin Plastic DIP Package



24 pin Plastic Flat Package

A0-A3:	Address input
D0-D3:	Data input/output
$\overline{CS0}$, $\overline{CS1}$	CHIP SELECTS 0, 1
$\overline{RD}$:	READ enable
$\overline{WR}$:	WRITE enable
ALE:	Address latch enable
STD.P:	Standard pulse output
XT, $\overline{XT}$:	XTAL oscillator input/output
VDD:	+5V supply
VSS:	ground

REGISTER TABLE

Address Input	Address Input				Register Name	Data				Count value	Description
	A_3	A_2	A_1	A_0		D_3	D_2	D_1	D_0		
0	0	0	0	0	S_1	S_8	S_4	S_2	S_1	0 ~ 9	1-second digit register
1	0	0	0	1	S_{10}	*	S_{40}	S_{20}	S_{10}	0 ~ 5	10-second digit register
2	0	0	1	0	MI_1	mi_8	mi_4	mi_2	mi_1	0 ~ 9	1-minute digit register
3	0	0	1	1	MI_{10}	*	mi_{40}	mi_{20}	mi_{10}	0 ~ 5	10-minute digit register
4	0	1	0	0	H_1	h_8	h_4	h_2	h_1	0 ~ 9	1-hour digit register
5	0	1	0	1	H_{10}	*	PM/AM	h_{20}	h_{10}	0 ~ 2 or 0 ~ 1	PM/AM, 10-hour digit register
6	0	1	1	0	D_1	d_8	d_4	d_2	d_1	0 ~ 9	1-day digit register
7	0	1	1	1	D_{10}	*	*	d_{20}	d_{10}	0 ~ 3	10-day digit register
8	1	0	0	0	MO_1	mo_8	mo_4	mo_2	mo_1	0 ~ 9	1-month digit register
9	1	0	0	1	MO_{10}	*	*	*	MO_{10}	0 ~ 1	10-month digit register
A	1	0	1	0	Y_1	y_8	y_4	y_2	y_1	0 ~ 9	1-year digit register
B	1	0	1	1	Y_{10}	y_{80}	y_{40}	y_{20}	y_{10}	0 ~ 9	10-year digit register
C	1	1	0	0	W	*	w_4	w_2	w_1	0 ~ 6	Week register
D	1	1	0	1	C_D	30 sec. ADJ	IRQ FLAG	BUSY	HOLD	–	Control Register D
E	1	1	1	0	C_E	t_1	t_0	ITRPT /STND	MASK	–	Control Register E
F	1	1	1	1	C_F	TEST	24/12	STOP	REST	–	Control Register F

REST = RESET
ITRPT/STND = INTERRUPT/STANDARD

Note 1) – Bit * does not exist (unrecognized during a write and held at "0" during a read).
Note 2) – Be sure to mask the AM/PM bit when processing 10's of hour's data.
Note 3) – BUSY bit is read only. The IRQ FLAG bit can only be set to a "0". Setting the IRQ FLAG to a "1" is done by hardware.

Figure 1. Register Table

OSCILLATOR FREQUENCY DEVIATIONS

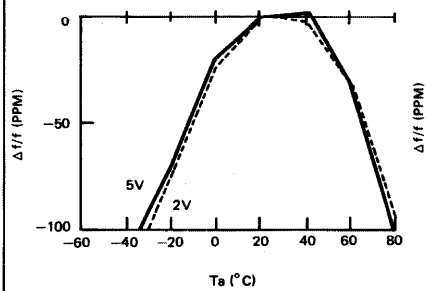


Figure 2. Frequency Deviation (PPM) vs Temperature

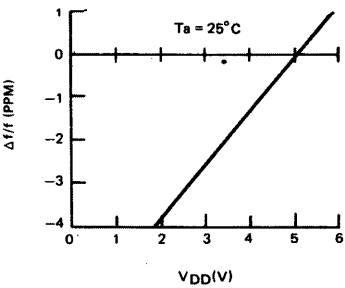
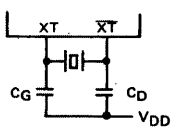


Figure 3. Frequency Deviation (PPM) vs Voltage

Note: 1. The graphs above showing frequency deviation vs temperature/voltage are primarily characteristic of the MSM6242 with the oscillation circuit described below.



Crystal: Type N_6, P_3 by kinseki (32.768 KHz)

C_G, C_D: 22pF (Temperature Characteristics: 0)

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	Ta = 25°C	−0.3~ 7	V
Input Voltage	V_I		GND − 0.3~V_{DD} + 0.3	V
Output Voltage	V_O		GND − 0.3~V_{DD} + 0.3	V
Storage Temperature	T_{STG}		−55~ +150	°C

OPERATING CONDITIONS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	–	4 ~ 6	V
Standby Supply Voltage	V_{BAK}	–	2 ~ 6	
Crystal Frequency	$f_{(XT)}$	–	32.768	kHz
Operating Temperature	T_{OP}	–	−30~+85	°C

D.C. CHARACTERISTICS

V_{DD} = 5V ± 10%, T_A = −30 ~ +85

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable Terminal
"H" Input Voltage	$V_{IH}1$	–	2.2	–	–	V	All input terminals except CS_1
"L" Input Voltage	$V_{IL}1$	–	–	–	0.8		
Input Leak Current	$I_{LK}1$	V_I = V_{DD}/0V	–	–	1/−1	μA	Input terminals other than D_0 ~ D_3
Input Leak Current	$I_{LK}2$		–	–	10/−10		D_0 ~ D_3
"L" Output Voltage	$V_{OL}1$	I_{OL} = 2.5mA	–	–	0.4	V	D_0 ~ D_3
"H" Output Voltage	V_{OH}	I_{OH} = −400μA	2.4	–	–		
"L" Output Voltage	$V_{OL}2$	I_{OL} = 2.5mA	–	–	0.4	V	STD.P
OFF Leak Current	I_{OFFLK}	V = V_{DD}/0V	–	–	10	μA	
Input Capacitance	C_I	Input frequency 1MHz	–	5	–	PF	All input terminals
Current Consumption	$I_{DD}1$	$f_{(xt)}$ = 32.768 KHz, T_a=25°C, V_{DD} = 5V	–	–	30	μA	V_{DD}
Current Consumption	$I_{DD}2$	$f_{(xt)}$ = 32.768 KHz, T_a=25°C, V_{DD} = 2V	–	–	10		
"H" Input Voltage	$V_{IH}2$	V_{DD} = 2~5.5V	4/5V_{DD}	–	–	V	CS_1
"L" Input Voltage	$V_{IL}2$		–	–	1/5V_{DD}		

SWITCHING CHARACTERISTICS

(1) WRITE mode (ALE = V_{DD})

(V_{DD} = 5V ± 10% = Ta = −30 ~ +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
CS_1 Set up Time	t_{C1S}	–	1000	–	ns
CS_1 Hold Time	t_{C1H}	–	1000	–	
Address Stable Before WRITE	t_{AW}	–	100	–	
Address Stable After WRITE	t_{WA}	–	10	–	
WRITE Pulse Width	t_{WW}	–	250	–	
Data Set up Time	t_{DS}	–	180	–	
Data Hold Time	t_{DH}	–	10	–	

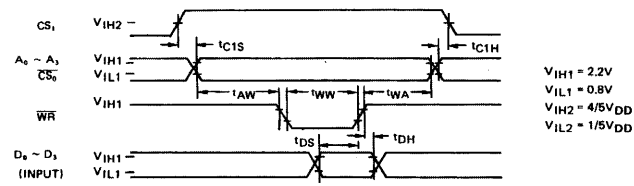


Figure 4. Write Cycle – (ALE = VDD)

(2) WRITE mode (With use of ALE)

(V_{DD} = 5 V ± 10%, Ta = −3C)

Parameter	Symbol	Condition	Min.	Max.	Unit
CS_1 Set up Time	t_{CIS}	–	1000	–	ns
Address Set up Time	t_{AS}	–	50	–	
Address Hold Time	t_{AH}	–	50	–	
ALE Pulse Width	t_{AW}	–	80	–	
ALE Before WRITE	t_{ALW}	–	0	–	
WRITE Pulse Width	t_{WW}	–	250	–	
ALE After WRITE	t_{WAL}	–	50	–	
DATA Set up Time	t_{DS}	–	180	–	
DATA Hold Time	t_{DH}	–	10	–	
CS_1 Hold Time	t_{C1H}	–	1000	–	

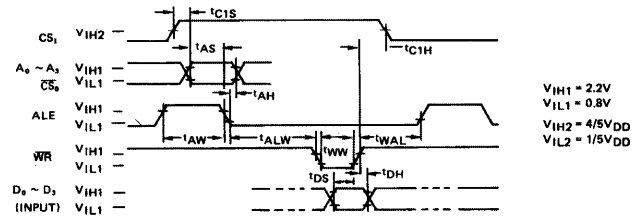


Figure 5. Write Cycle – (With Use of ALE)

(3) READ mode (ALE = V_{DD})

(V_{DD} = 5V ± 10%, Ta = –30 ~ +85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
$\overline{CS_1}$ Set up Time	t_{C1S}	–	1000	–	ns
CS_1 Hold Time	t_{C1H}	–	1000	–	
Address Stable Before READ	t_{AR}	–	80	–	
Address Stable After READ	t_{RA}	–	0	–	
$\overline{RD}$ to Data	t_{RD}	C_L = 150pF	–	280	
Data Hold	t_{DR}	–	0	–	

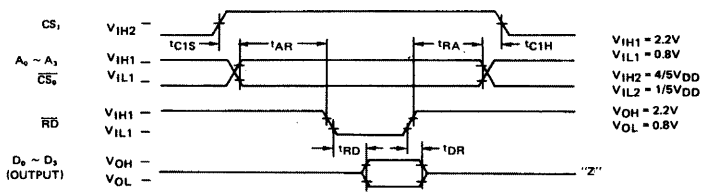


Figure 6. Read Cycle – (ALE = VDD)

(4) READ mode (With use of ALE)

(V_{DD} = 5V ±10%, Ta = −30~+85°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
CS_1 Set up Time	t_{C1S}	–	1000	–	ns
Address Set up Time	t_{AS}	–	50	–	
Address Hold Time	t_{AH}	–	50	–	
ALE Pulse Width	t_{AW}	–	80	–	
ALE Before READ	t_{ALR}	–	0	–	
ALE after READ	t_{RAL}	–	0	–	
RD to Data	t_{RD}	C_L = 150pF	–	280	
DATA Hold	t_{DR}	–	0	–	
CS_1 Hold Time	t_{C1H}	–	1000	–	

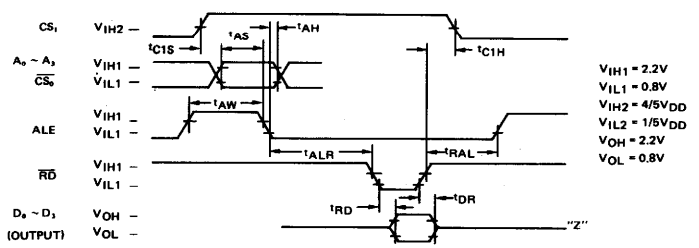
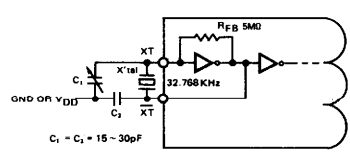


Figure 7. Read Cycle – (With Use of ALE)

PIN DESCRIPTION

Name	Pin No. RS	Pin No. GS	Description
D_0	14	19	Data Input/Output pins to be directly connected to a microcontroller bus for reading and writing of the clock/calendar's registers and control registers. D0 = LSB and D3 = MSB.
D_1	13	16	
D_2	12	15	
D_3	11	14	
A_0	4	5	Address input pin for use by a microcomputer to select internal clock/calendar's registers and control registers for Read/Write operations (See Function Table Figure 1). Address input pins A0-A3 are used in combination with ALE for addressing registers.
A_1	5	7	
A_2	6	9	
A_3	7	10	
ALE	3	4	Address Latch Enable pin. This pin enables writing of address data when ALE = 1 and $\overline{CS0}$ = 0; address data is latched when ALE = 0 Microcontroller/Microprocessors having an ALE output should connect to this pin; otherwise it should be connected at V_{DD}.
$\overline{WR}$	10	13	Writing of data is performed by this pin. When CS_1 = 1 and $\overline{CS_0}$ = 0, $D_0 \sim D_3$ data is written into the register at the rising edge of $\overline{WR}$.
$\overline{RD}$	8	11	Reading of register data is accomplished using this pin. When CS_1 = 1, $\overline{CS_0}$ = 0 and $\overline{RD}$ = 0, the data of the register is output to $D_0 \sim D_3$. If both $\overline{RD}$ and $\overline{WR}$ are set at 0 simaltanuously, $\overline{RD}$ is to be inhibited.
$\overline{CS_0}$	2	2	Chip Select Pins. These pins enable/disable ALE, $\overline{RD}$ and $\overline{WR}$ operation. $\overline{CS_0}$ and ALE work in combination with one another, while CS_1 work independent with ALE. CS_1 must be connected to power failure detection as shown in Figure 18.
CS_1	15	20	
STD.P	1	1	Output pin of N-CH OPEN DRAIN type. The output data is controlled by the D_1 data content of C_E register. This pin has a priority to $\overline{CS_0}$ and CS_1. Refer to Figure 9 and FUNCTIONAL DESCRIPTION OF REGISTERS.
XT	16	22	32.768 kHz crystal is to be connected to these pins. When an external clock of 32.768 kHz is to be used for MSM6242's oscillation source, either CMOS output or pull-up TTL output is to be input from XT, while $\overline{XT}$ should be left open.
$\overline{XT}$	17	23	
V_{DD}	18	24	Power supply pin. +2 ~ +6V power is to be applied to this pin.
GND	9	12	Ground pin.



The impedance of the crystal should be less than 30kΩ

Figure 8. Oscillator Circuit

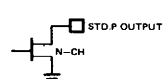


Figure 9.

FUNCTIONAL DESCRIPTION OF REGISTERS

■ $S_1, S_{10}, MI_1, MI_{10}, H_1, H_{10}, D_1, D_{10}, M\overline{O}_1, M\overline{O}_{10}, Y_1, Y_{10}, W$

a) These are abbreviations for SECOND1, SECOND10, MINUTE1, MINUTE10, HOUR1, HOUR10, DAY1, DAY10, MONTH1, MONTH10, YEAR1, YEAR10, and WEEK. These values are in BCD notation.

b) All registers are logically positive. For example, (S8, S4, S2, S1) = 1001 which means 9 seconds.

c) If data is written which is out of the clock register data limits, it can result in erroneous clock data being read back.

d) PM/AM, h_{20}, h_{10}
In the mode setting of 24-hour mode, PM/AM bit is ignored, while in the setting of 12-hour mode h_{20} is to be set. Otherwise it causes a discrepancy. In reading out the PM/AM bit in the 24-hour mode, it is continuously read out as 0. In reading out h_{20} bit in the 12-hour mode, 0 is written into this bit first, then it is continuously read out as 0 unless 1 is being written into this bit.

e) Registers Y1, Y10, and Leap Year. The MSM6242 is designed exclusively for the Christian Era and is capable of identifying a leap year automatically. The result of the setting of a non-existant day of the month is shown in the following example: If the date February 29 or November 31, 1985, was written, it would be changed automatically to March 1, or December 1, 1985 at the exact time at which a carry pulse occurs for the day's digit.

f) The Register W data limits are 0–6 (Table 1 shows a possible data definition).

TABLE 1

W_4	W_2	W_1	Day of Week
0	0	0	Sunday
0	0	1	Monday
0	1	0	Tuesday
0	1	1	Wednesday
1	0	0	Thursday
1	0	1	Friday
1	1	0	Saturday

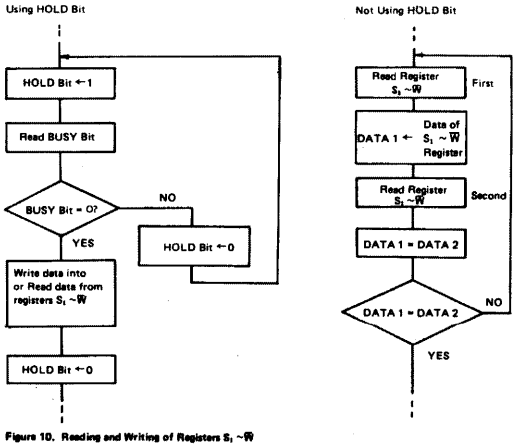
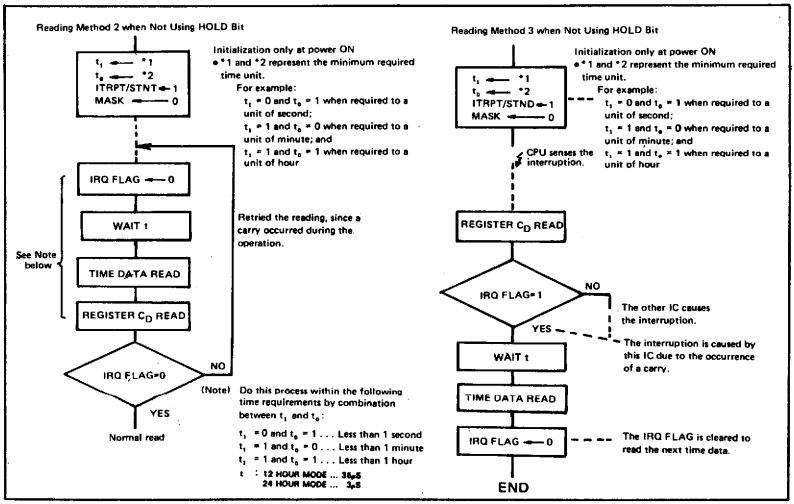


Figure 10. Reading and Writing of Registers $S_1 \sim \overline{W}$



■ CD REGISTER (Control D Register)

a) HOLD (D0) – Setting this bit to a "1" inhibits the 1Hz clock to the S1 counter, at which time the Busy status bit can be read. When Busy = 0, register's $S_1 \sim \overline{W}$ can be read or written. During this procedure if a carry occurs the S1 counter will be incremented by 1 second after HOLD = 0 (this condition is guaranteed as long as HOLD = 1 does not exceed 1 second in duration). If CS1 = 0 then HOLD = 0 irrespective of any condition.

b) BUSY (D1) – Status bit which shows the interface condition with microcontroller/microprocessors. As for the method of writing into and reading from $S_1 \sim \overline{W}$ (address $\phi \sim C$), refer to the flow chart described in Figure 10.

c) IRQ FLAG (D2) – This status bit corresponds to the output level of the STD.P output. When STD.P = 0, then IRQ = 1; when STD.P=1, then IRQ = 0. The IRQ FLAG indicates that an interrupt has occurred to the microcomputer if IRQ = 1. When D0 of register C_E (MASK) = 0, then the STD.P output changes according to the timing set by D3 (t_1) and D2 (t_0) of register E. When D1 of register E (ITRPT/STND) = 1 (interrupt mode), the STD.P output remains low until the IRQ FLAG is written to a "0". When IRQ = 1 and timing for a new interrupt occurs, the new interrupt is ignored. When ITRPT/STND = 0 (Standard Pulse Output mode) the STD.P output remains low until either "0" is written to the IRQ FLAG; otherwise, the IRQ FLAG automatically goes to "0" after 7.8125 ms.

When writing the HOLD or 30 second adjust bits of register D, it is necessary to write the IRQ FLAG bit to a "1".

d) ±30 ADJ (D3) – When 30-second adjustment is necessary, a "1" is written to bit D3 during which time the internal clock registers should not be read from or written to 125μs after bit D3 = 1 it will automatically return to a "0", and at that time reading or writing of registers can occur.

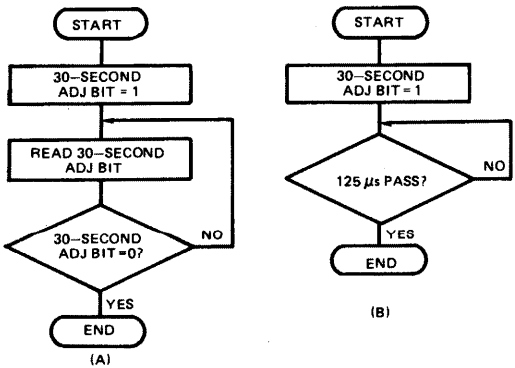


Figure 11. Writing 30-Second Adj. bit (Two Ways A, B)

■ CE REGISTER (Control E Register)

a) MASK (D0) – This bit controls the STD.P output. When MASK = 1, then STD.P = 1 (open); when MASK = 0, then STD.P = output mode. The relationship between the MASK bit and STD.P output is shown Figure 12.

b) INTRPT/STND (D1) – The INTRPT/STND input is used to switch the STD.P output between its two modes of operation, interrupt and Standard timing waveforms. When INTRPT/STND 0 a fixed cycle waveform with a low-level pulse width of 7.8125 ms is present at the STD.P output. At this time the MASK bit must equal 0, while the period in either mode is determined by T0(D2) and T1(D3) of Register E.

c) T0 (D2), T1 (D3) – These two bits determine the period of the STD.P output in both Interrupt and Fixed timing waveform modes. The tables below show the timing associated with the T0, T1 inputs as well as their relationship to INTRPT/STND and STD.P.

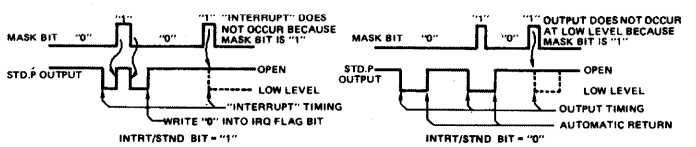
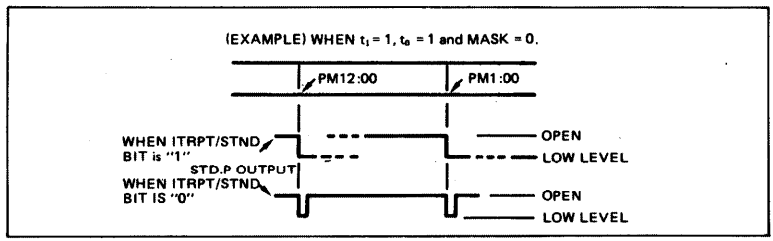


Figure 12.

t_1	t_0	Period	Duty CYCLE of "0" level when ITRPT/STND bit is "0".
0	0	1/64 second	1/2
0	1	1 second	1/128
1	0	1 minute	1/7680
1	1	1 hour	1/460800

TABLE 2

The timing of the STD.P output designated by T1 and T0 occurs the moment that a carry occurs to a clock digit.



d) The low-level pulse width of the fixed cycle waveform (ITRPT/STND = 0) is 7.8125 ms independent of T0/T1 inputs.

e) The fixed cycle waveform mode can be used for adjustment of the oscillator frequency time base. (See Figure 14).

f) During ±30 second adjustment a carry can occur that will cause the STD.P output to go low when T0/T1 = 1,0 or 1,1. However, when T1/T0 = 0, 0 and ITRPT/STND = 0, carry does not occur and the STD.P output resumes normal operation.

g) The STD.P output is held (frozen) at the point at which STOP = 1 while ITRPT/STND = 0.

h) No STD.P output change occurs as a result of writing data to registers S1 ~ H1.

■ C_F REGISTER (Control F Register)

a) REST (D0) – "RESET" — This bit is used to clear the clock's internal divider/counter of less than a second. When REST = 1, the counter is Reset for the duration of REST. In order to release this counter from Reset, a "0" must be written to the REST bit. If $\overline{CSO}$ = 0 then REST = 0 automatically.

b) STOP (D1) – The STOP FLAG Only inhibits carries into the 8192Hz divider stage. There may be up to 122μs delay before timing starts or stops after changing this flag; 1 = STOP/0 = RUN.

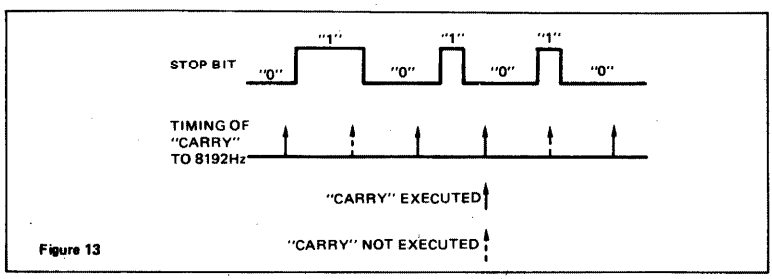


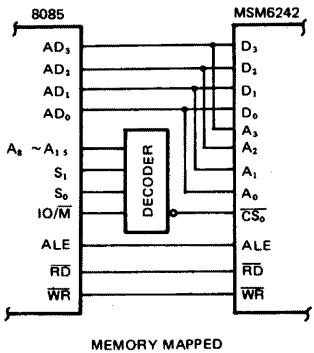
Figure 13

c) 24/12 (D2) – This bit is for selection of 24/12 hour time modes. If D2 = 1—24 hour mode is selected and the PM/AM bit is invalid. If D2 = 0—12 hour mode is selected and the PM/AM bit is valid.

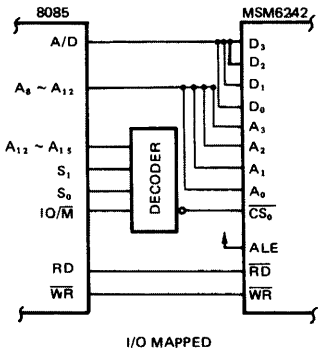
"24 HOUR/ 12 HOUR" — Setting of the 24/12 hour bit is as follows:
1) REST bit = 1
2) 24/12 hour bit = 0 or 1
3) REST bit = 0
* REST bit must = 1 to write to the 24/12 hour bit.

d) TEST (d3) – When the TEST flag is a "1", the input to the SECONDS counter comes from the counter/divider stage instead of the 15th divider stage. This makes the SECONDS counter count at 5.4163KHz instead of 1Hz. When TEST = 1 (Test Mode) the STOP & REST (Reset) flags do not inhibit internal counting. When Hold = 1 during Test (Test = 1) internal counting is inhibited; however, when the HOLD FLAG goes inactive (Hold = 0) counter updating is not guaranteed.

TYPICAL APPLICATION INTERFACE WITH MSM6242 AND MICROCONTROLLERS



MEMORY MAPPED



I/O MAPPED

Figure 15.

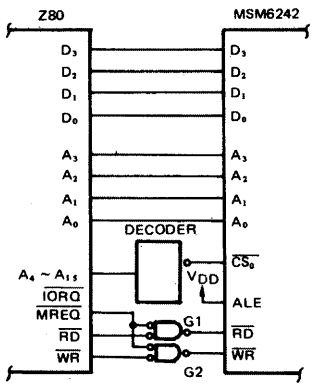


Figure 16.

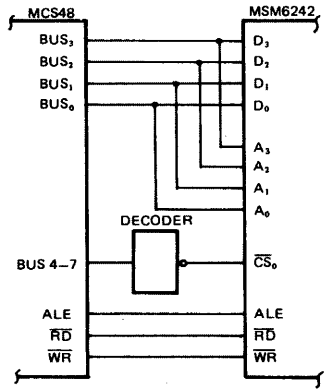


Figure 17.

TYPICAL APPLICATIONS – INTERFACE WITH MSM80C49

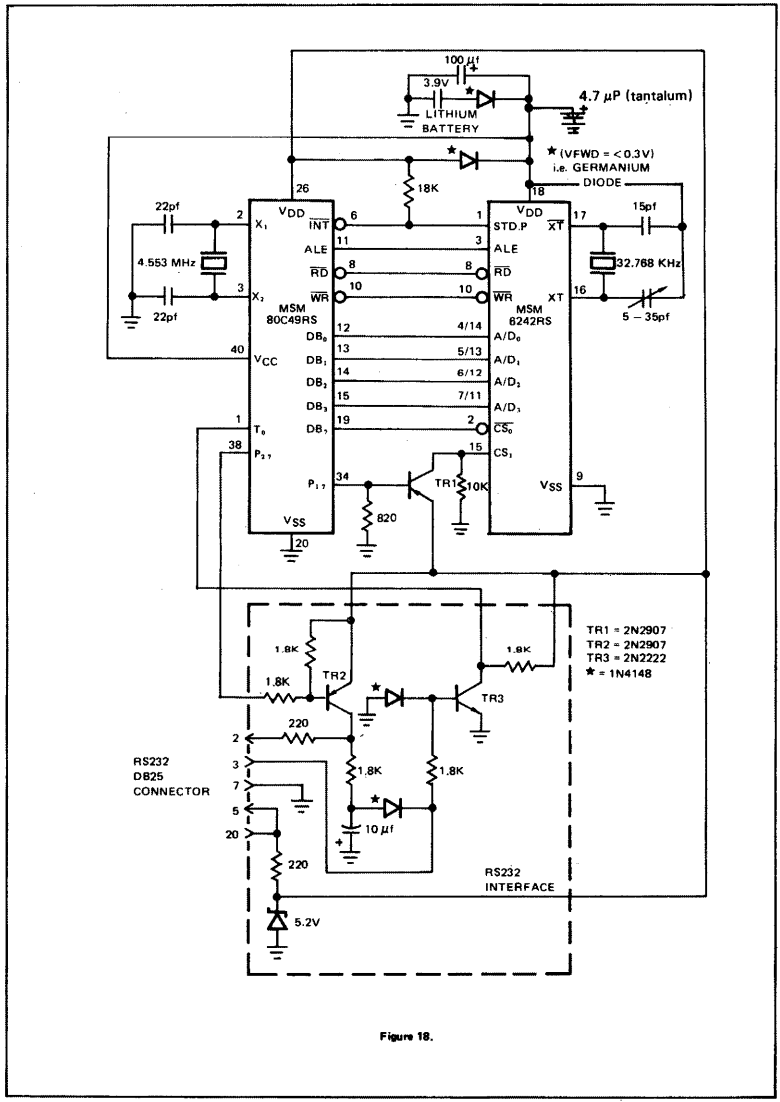
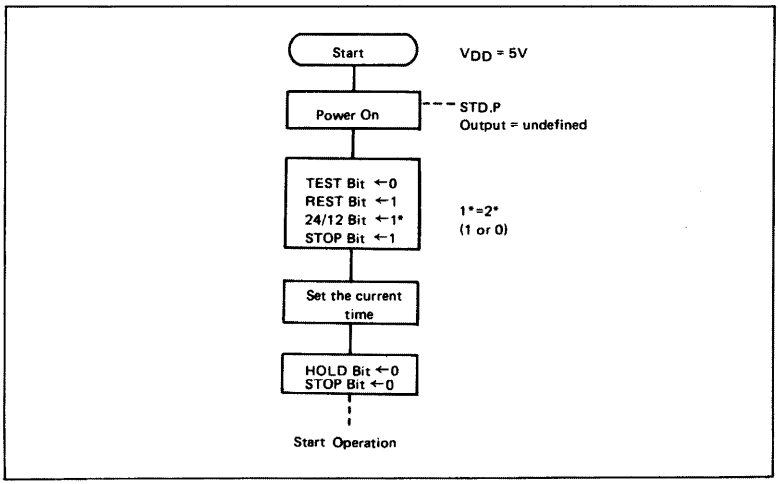


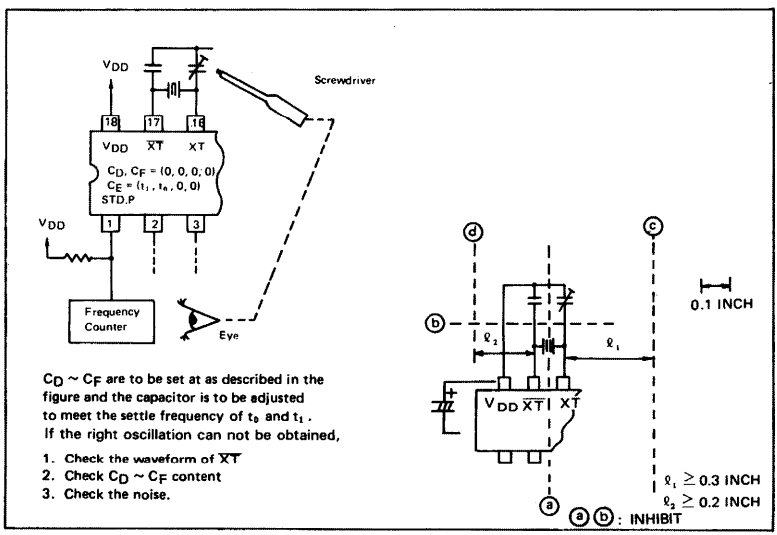
Figure 18.

APPLICATION NOTE

1. Power Supply



2. Adjustment of Frequency



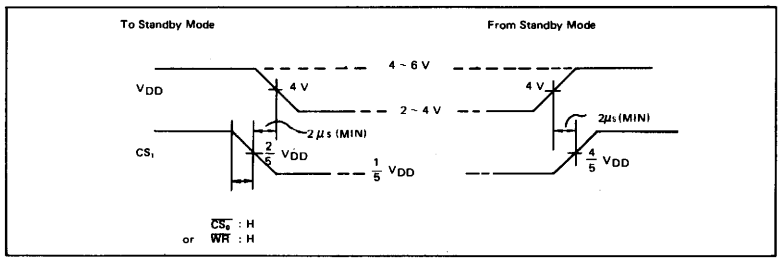
3. CH_1 (Chip Select)

V_{IH} and V_{IL} of CH_1 has 3 functions.

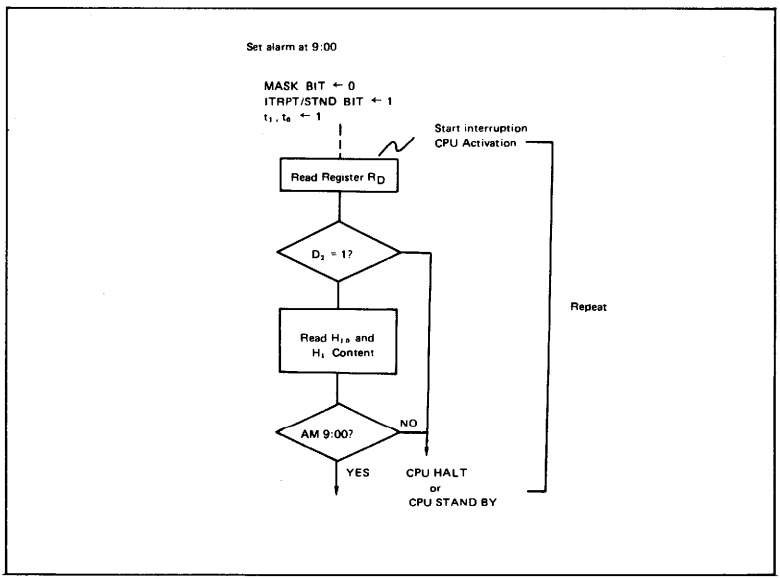
a) To accomplish the interface with a microcontroller/microprocessor.
b) To inhibit the control bus, data bus and address bus and to reduce input gate pass current in the stand-by mode.
c) To protect internal data when the mode is moved to and from standby mode.

To realize the above functions:

a) More than 4/5 V_{DD} should be applied to the MSM6242 for the interface with a microcontroller/microprocessor in 5V operation.
b) In moving to the standby mode, 1/5 V_{DD} should be applied so that all data buses should be disabled. In the standby mode, approx. 0V should be applied.
c) To and from the standby mode, obey following Timing chart.



4. Set STD.P at arlarm mode



TYPICAL APPLICATION – POWER SUPPLY CIRCUIT

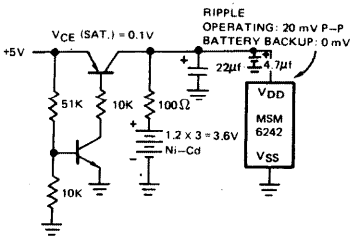


Figure 19.

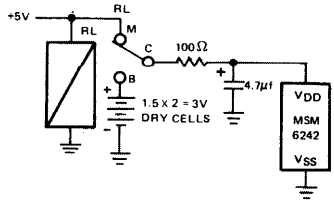


Figure 20.

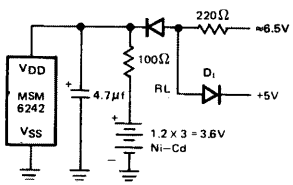
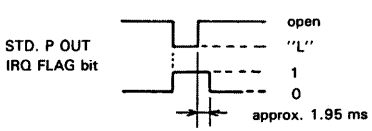


Figure 21.

4.7 μF: tantalum

SUPPLEMENTARY DESCRIPTION

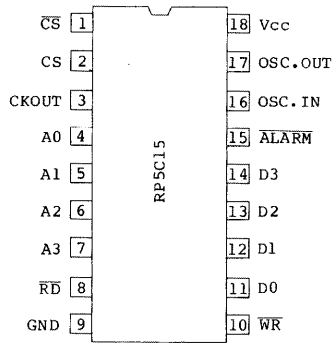
- When "0" is written to the IRQ FLAG bit, the IRQ FLAG bit is cleared. However, if "0" is assigned to the IRQ FLAG bit when written to the other bits, the 30-sec ADJ bit and the HOLD bit, the IRQ FLAG = 1 and was generated before the writing and IRQ FLG = 1 generated in a moment then will be cleared. To avoid this, always set "1" to the IRQ FLAG unless "0" is written to it intentionally. By writing "1" to it, the IRQ FLAG bit does not become "1".
- Since the IRQ FLAG bit becomes "1" in some cases when rewriting either of the t_1, t_0, or ITRPT/STND bit of register C_E, be sure to write "0" to the IRQ FLAG bit after writing to make valid the IRQ FLAG = 1 to be generated after it.
- The relationship between SDT. P OUT and IRQ FLAG bit is shown below:



Specifications of RP5C15

Outline:

The RP5C15 is a real-time clock that can be connected directly to the bus of microprocessors using not only the 8-bit CPU such as 8085, Z80, 6809, 6502 but also the 16-bit CPU such as 8086, Z8000, 68000 or others. Time can then be written to or read from the clock in the same way as writing to or reading from RAM. As well as calendar and time counters and alarm function allowing battery backup.

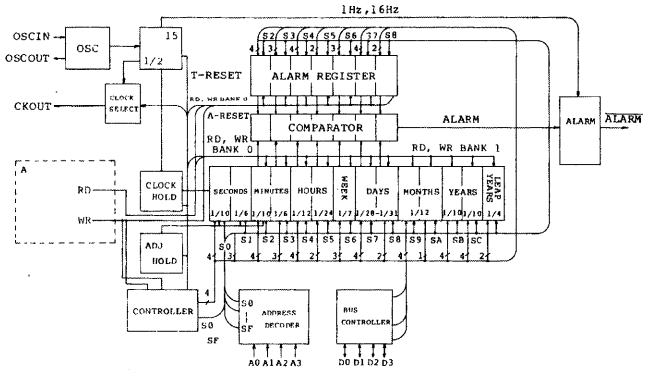


Pin configuration

Featrues:

* Direct connection to CPU and Hi-speed access
* 4-bit bidirectional bus D0~D3
* 4-bit address inputs A0~A3
* Internal counters for time (hours, min., sec.) and date (100 years, leap years, months, days, and days-of-the-week)
* All clock data expressed in BCD code
* ±30 sec. adjustment function
* Provision for battery backup
* Choice of standard clock from 16 kHz, 1.024 kHz, 128 kHz, 16 Hz, 1 Hz, 1/60 Hz
* Alarm signal, 16 Hz clock signal or 1 Hz clock signal output

Block diagram



Absolute maximum ratings (See Note 1)

Symbol	Item	Measurement conditions	Values	Units
VCC	Supply voltage	GND = 0	-0.3 ~ +7	V
VI	Input voltage	GND = 0	-0.3 ~ VCC+0.3	V
VC	Output voltage	GND = 0	-0.3 ~ VCC+0.3	V
PD	Maximum power dissipation	Ta = 25°C	600	mW
TOPG	Ambient temp. during operation		-20 ~ 70	°C
TSTG	Ambient temp. during storage		-40 ~ 125	°C

(Note 1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended operating conditions

Ta = -20°C to 70°C unless otherwise specified.

Symbol	Item	Values			Units
		Min.	Typ.	Max.	
VCC	Supply voltage	4.5	5.0	5.5	V
VDH	Data backup voltage	2.0		5.5	V
fxt	Oscillation frequency of crystal oscillator		32.768		kHz

DC characteristics during normal operation

Ta = -20°C to 70°C, Vcc = 5V ±10% unless otherwise specified.

Symbol	Item	Measurement conditions	Values			Units	Remarks
			Min.	Typ.	Max.		
VIH	"H" input voltage		2.0		Vcc+0.3	V	
VIL	"L" input voltage		-0.3		0.8	V	
VOH	"H" output voltage	IOH=-400μA	2.4			V	Except for pin 3,15
VOL	"L" output voltage	IOL=2mA			0.4	V	
IILK	Input leakage current	VIN=0 ~ VCC	-10		10	μA	
IFLK	Floating leakage current	VFV=0 ~ VCC	-10		10	μA	
IDDI	Current consumed during operation	(Note 2)			300	μA	

(Note 2) Vcc = 5V; R/W signal f =100kHz; Input terminals, Vcc or GND; Output terminals on no-load; Crystal oscillator (32.768kHz); Measurement temp. (25°C).

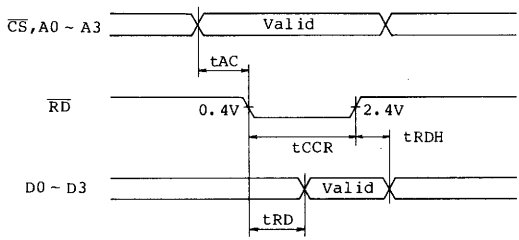
AC electrical characteristics

Ta=-20°C to 70°C, Vcc=5V±10% unless otherwise specified.

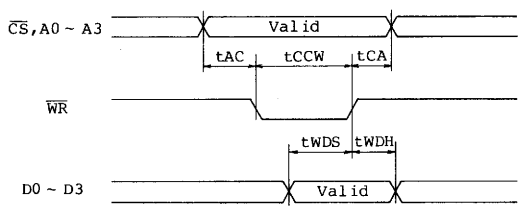
Symbol	Item	Measurement conditions	Values			Units	Remarks
			Min.	Typ.	Max.		
tAC	Address valid -- $\overline{RD}/\overline{WR}$ trailing edge		50			ns	$\overline{CS}$=low and address valid
tccR	$\overline{RD}$ pulse width		120		13000	ns	
tccW	$\overline{WR}$ pulse width		120		13000	ns	
tRD	$\overline{RD}$ trailing edge --data valid	(Note 1)			120	ns	
tcA	$\overline{RD}/\overline{WR}$ leading edge --address hold		10			ns	
tWDS	Write data setup time		100			ns	
tWDH	Write data hold time		20			ns	
tRDH	$\overline{RD}$ leading edge --data valid		10			ns	
tEN-DIS	Timer Enable-- Timer Disable		100			μs	
tADJ	Adjustment completion time				100	μs	
tAINH	Alarm data write inhibit time after alarm reset		100			μs	
tRCV	$\overline{RD}/\overline{WR}$ recovery time		1			μs	

Timing chart

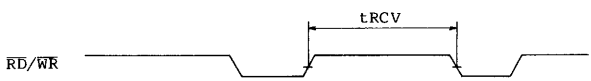
READ cycle (CS = "H")



WRITE cycle (CS = "H")



Others



Function of pins

Name of pin	No. of pin	Function
$\overline{CS}$ CS	1 2	External interface terminals. Valid when both CS = H and $\overline{CS}$ = L. CS is connected to the power-down detector of the peripheral circuitry, and $\overline{CS}$ to the address decoder of the CPU.
CKOUT	3	Output terminal for standard clock signal. Can take 8 different states depending on contents of CKOUT selection register. N-ch open drain output.
A0 ~ A3	4,5,6,7	Address input. Connected to address bus of CPU.
$\overline{RD}$	8	I/O control input. Set to low when data of RP5C15 is read. Low active input.
GND	9	OV
$\overline{WR}$	10	I/O control input. Set to low when data of RP5C15 is written. Low active input.
D0 ~ D3	11,12,13,14	Bidirectional bus. Connected directly to CPU data bus.
$\overline{ALARM}$	15	Output terminal for alarm signal and 1Hz/16Hz clock signals. N-ch open-drain output.
OSC IN	16	Connected to 32.768kHz crystal oscillator circuit.
OSC OUT	17	Connected to 32.768kHz crystal oscillator circuit.
VCC	18	+5V power supply

Address allocation

* "x" means "Don't care" when written, and always "0" when read out.
* Address 0~D: able to read to and write from, except for ADJUST register which can only be written to.
  Address E~F: "write" only (always "0" when read out)

Bank 0						Bank 1				
A_3~A_0	Contents	D_3	D_2	D_1	D_0	Contents	D_3	D_2	D_1	D_0
0	1-sec. counter					CKOUT selection register	X	CK2	CK1	CK0
1	10-sec. counter	X				Adjust register	X	X	X	Adjust
2	1-min. counter					Alarm 1-min. register				
3	10-min. counter	X				Alarm 10-min. register	X			
4	1-hour counter					Alarm 1-hour register				
5	10-hour counter	X	X			Alarm 10-hour register	X	X		
6	Day-of-the-week counter	X				Alarm day-of-the-week register	X			
7	1-day counter					Alarm 1-day register				
8	10-day counter	X	X			Alarm 10-day register	X	X		
9	1-month counter						X	X	X	X
A	10-month counter	X	X	X		$\overline{12}$/24 hour selector	X	X	X	
B	1-year counter					Leap-year counter	X	X		
C	10-year counter						X	X	X	X
D	Mode register	Timer EN	Alarm EN	X	Bank 1/0	Mode register	Timer EN	Alarm EN	X	Bank 1/0
E	Test register	Test 3	Test 2	Test 1	Test 0	Test register	Test 3	Test 2	Test 1	Test 0
F	Reset controller	$\overline{1Hz}$ $\overline{ON}$	$\overline{16Hz}$ $\overline{ON}$	Timer RESET	Alarm RESET	Reset controller	$\overline{1Hz}$ $\overline{ON}$	$\overline{16Hz}$ $\overline{ON}$	Timer RESET	Alarm RESET

CKOUT selection register

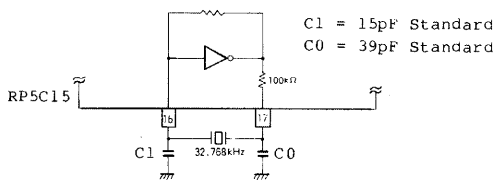
D3	D2	D1	D0	CKOUT	Remarks
X	0	0	0	"Z"	High-impedance
X	0	0	1	16.384kHz	Duty 50%
X	0	1	0	1.024kHz	Duty 50%
X	0	1	1	128Hz	Duty 50%
X	1	0	0	16Hz	Duty 50%
X	1	0	1	1Hz	↓Seconds counter increment. Duty 50%
X	1	1	0	1/60Hz	↓Minutes counter increment. Duty 50%
X	1	1	1	"L"	Low Level

Adjustment function

BANK 1 ADDRESS (A3,A2,A1,A0)=(0,0,0,1) DATA (D3,D2,D1,D0)=(X,X,X,1)	Second counter backs to 0 when it's adjusted 0 ~ 29 sec. If it's adjusted on 30 ~ 59 sec., the second counter goes up to 0 sec. and the minute counter shows the next minute.

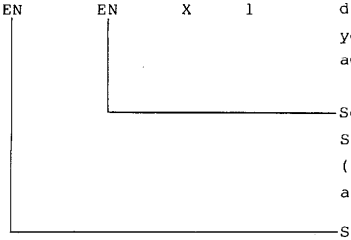
Oscillator circuit

Not required because an output ballast registor (Approx. 100kΩ) is used.



*Bank register (A3,A2,A1,A0) = (1,1,0,1) = D

D3	D2	D1	D0	
Timer EN	Alarm EN	X	0	BANK0:setting or rate time
		X	1	BANK1:setting or rate of Alarm data, 12/24 hour system, leap year, choice of CLKOUT, and adjustment



Set 1 to enable alarm output
Set 0 to disable alarm output
(16Hz/1Hz clock signals not affected)

Set 1 to start clock. Set 0 to stop seconds and subsequent counters.

*The leap-year counter registers a leap year when D1 = D0 = 0. It simultaneously counts with the year counter.

*The 12-hour/24-hour selector sets the 12-hour system when D0 = 0 and the 24-hour system when D0 = 1. PM or AM is selected when D1 in the 10-hour counter is 1 or 0, respectively.

*Reset controller 16Hz/1Hz clock register.

(A3,A2,A1,A0) = (1,1,1,1) = F

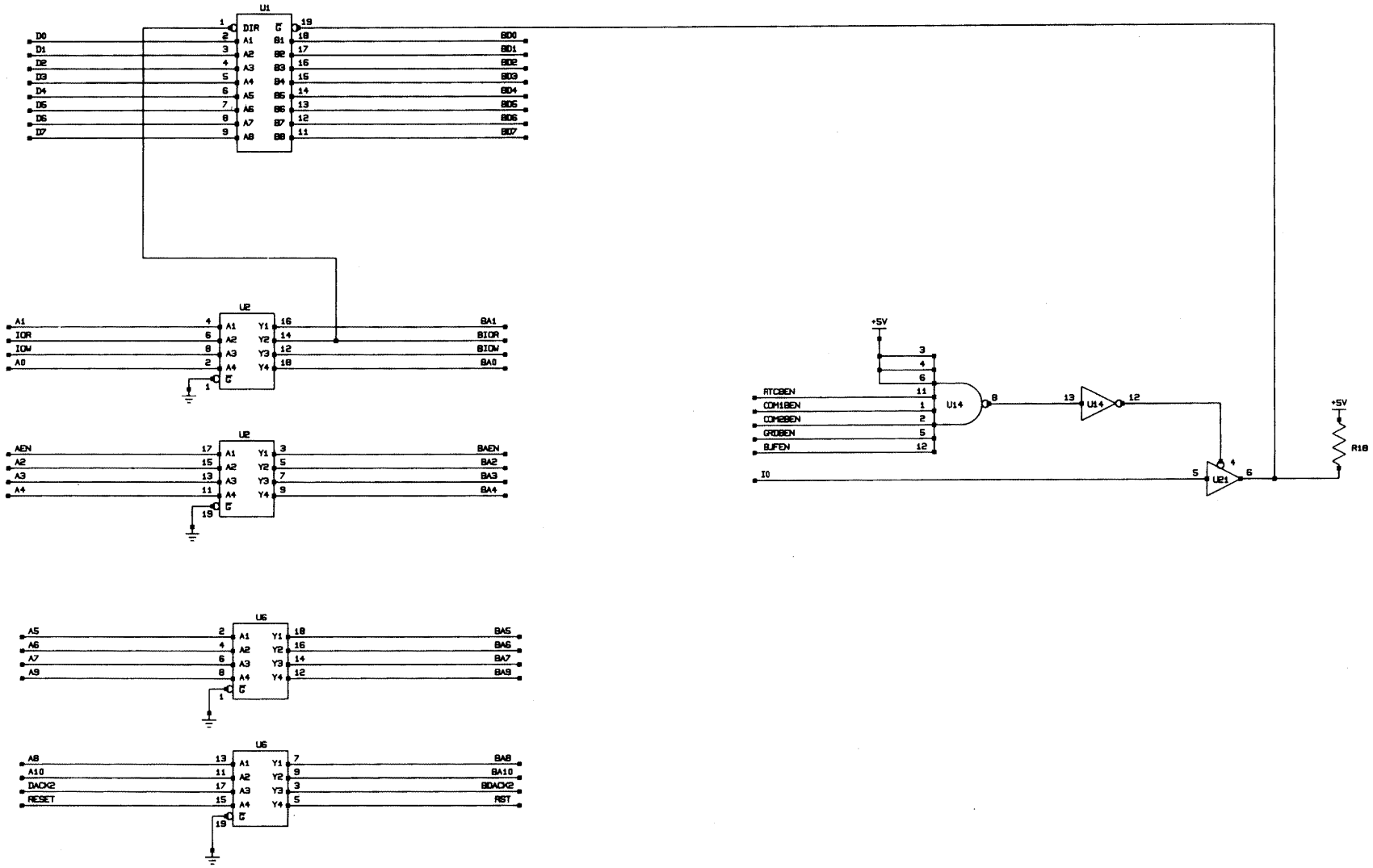
D0 = 1:resets all alarm register and internal Alarm F/Fs.
D1 = 1:dividers before seconds counter reset.
D2 = 0:switches on the 16Hz clock pulse generated from the ALARM terminal.
D3 = 0:switches on the 1Hz clock pulse generated from the ALARM terminal.

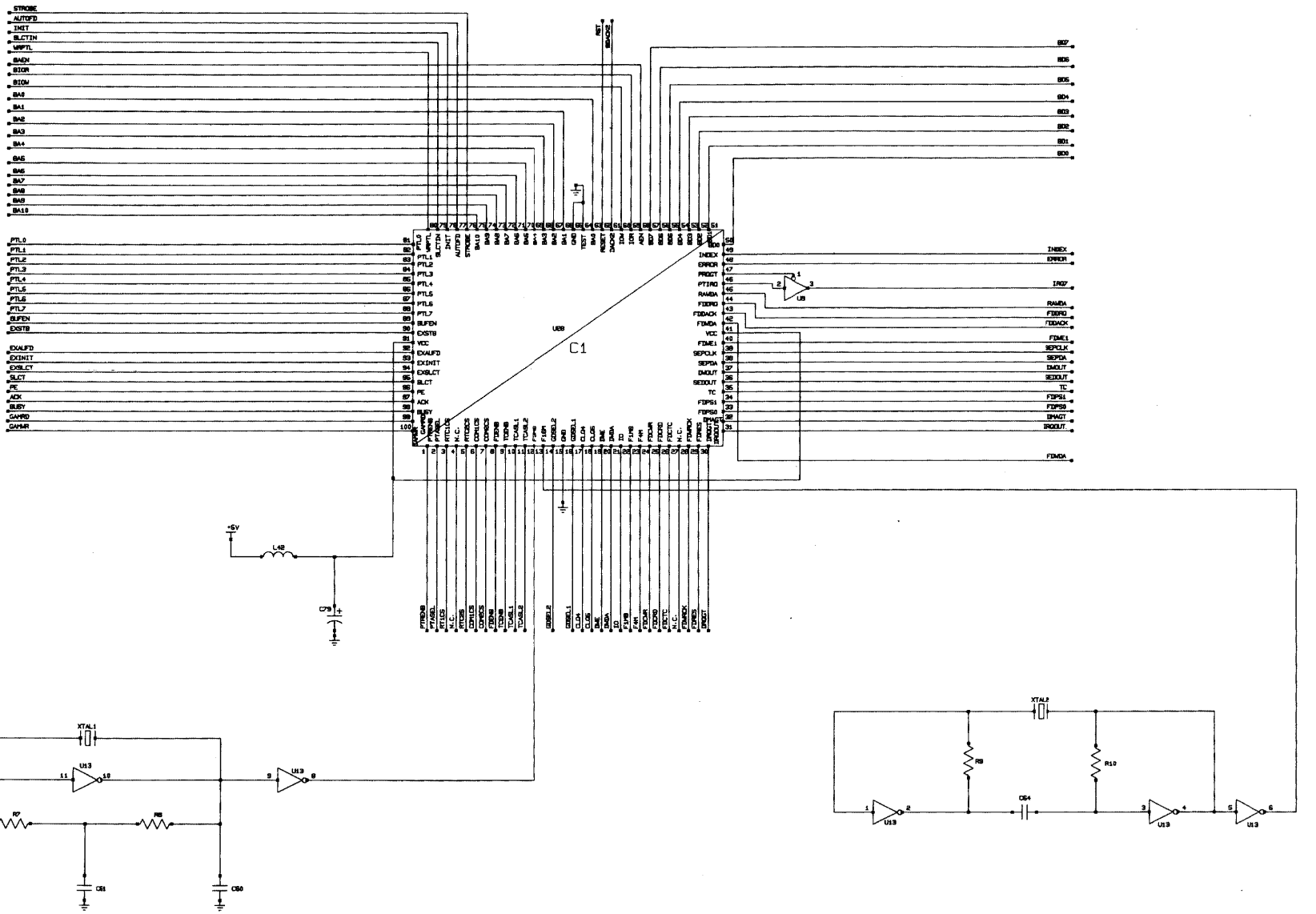
*Addresses 0 ~ D:able to read and write.

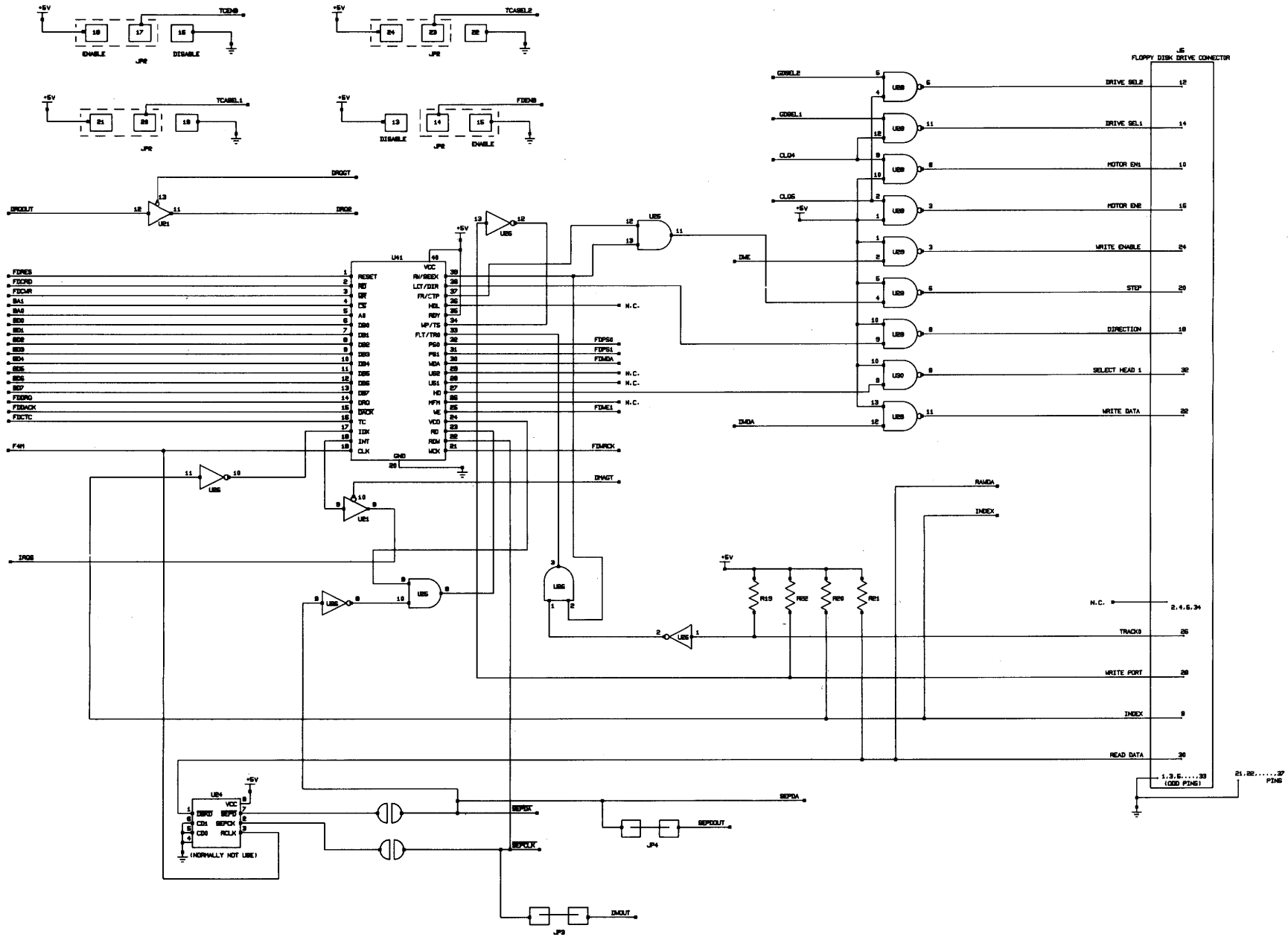
*Addresses E ~ F:only able to write and 0H always appears when read out.

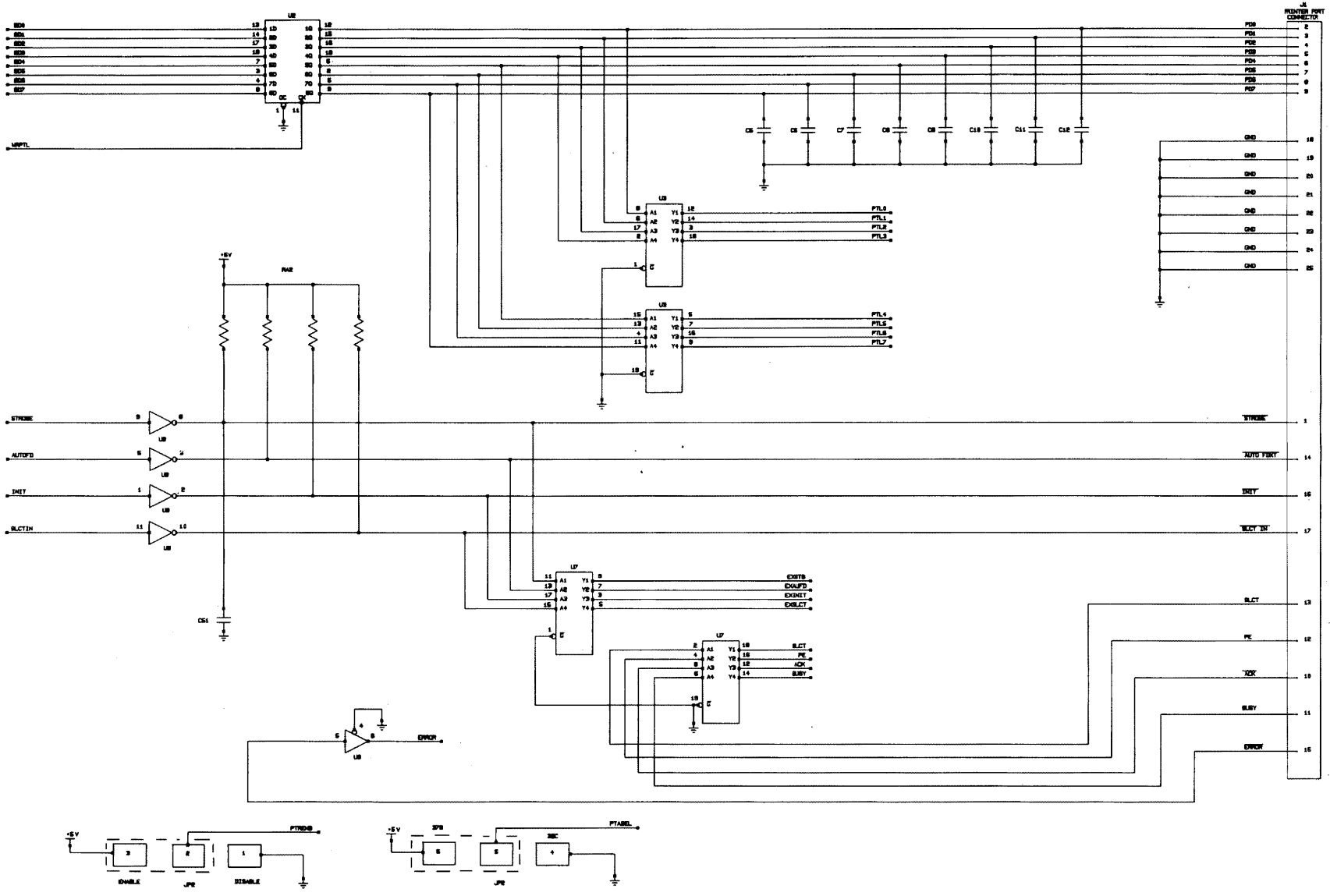
*TEST register (A3,A2,A1,A0) = (1,1,1,0) = E:use for inspections at Ricoh Co., Ltd. Normal watch function is achieved by setting of the data (D3,D2,D1,D0) = (0,0,0,0).

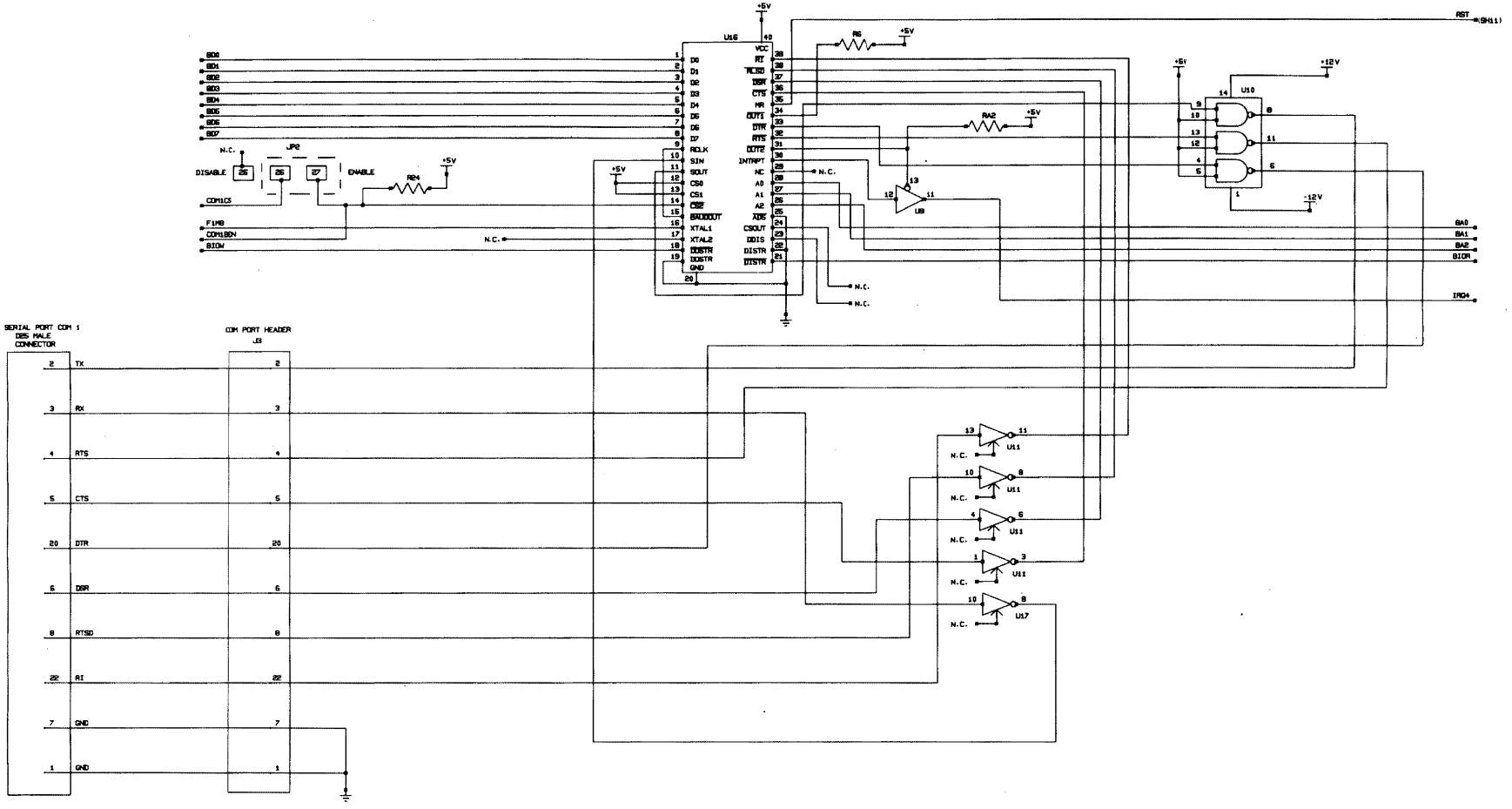
For details, refer to the Application Manual.

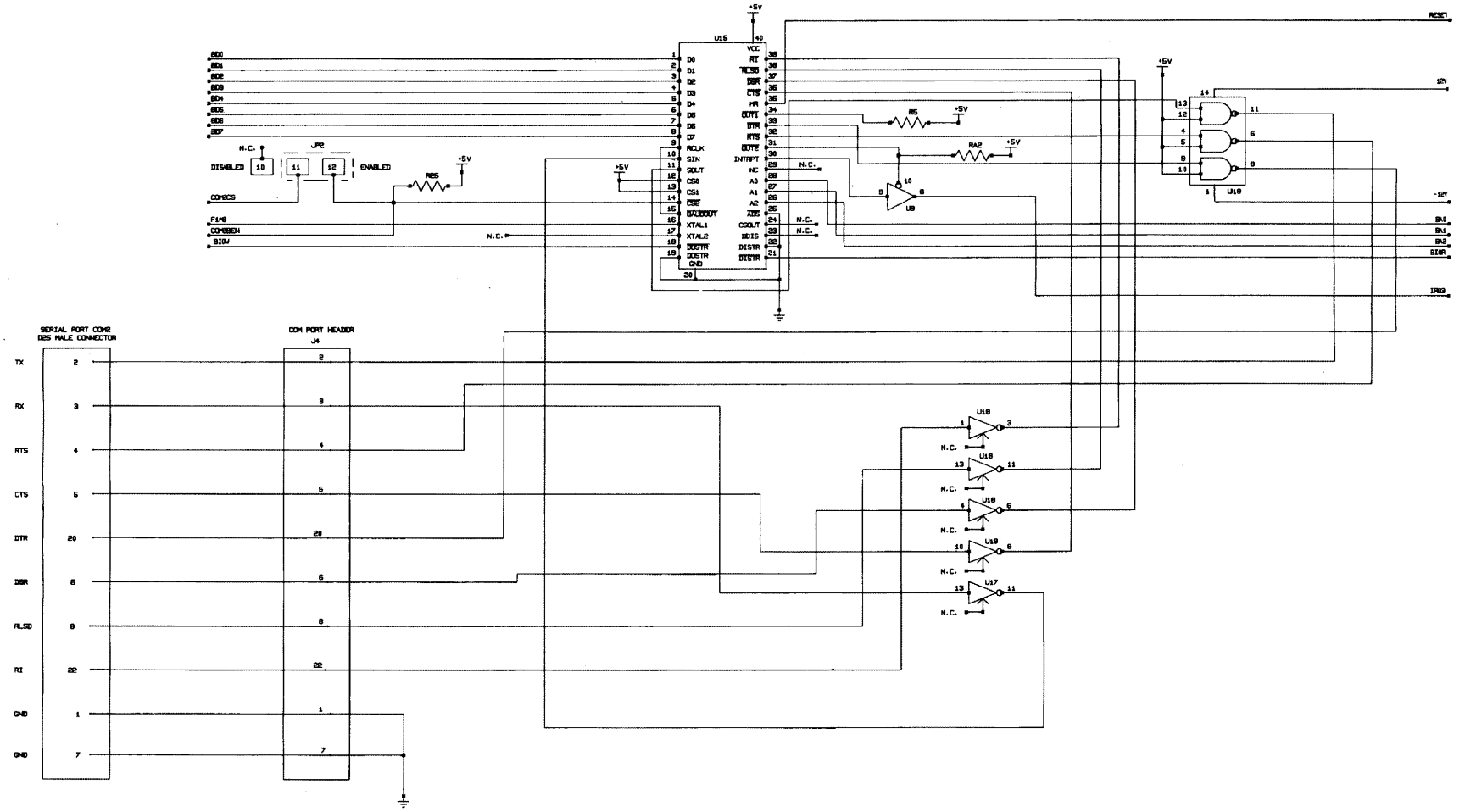

U1
DIR
D0
D1
D2
D3
D4
D5
D6
D7
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
U2
A1
IOR
IOW
A0
BA1
BIOR
BIOW
BA0
U2
AEN
A2
A3
A4
BAEN
BA2
BA3
BA4
U6
A5
A6
A7
A9
BA5
BA6
BA7
BA9
U6
A8
A10
DACK2
RESET
BA8
BA10
BDACK2
RST
+5V
RTCBEN
COM1BEN
COM2BEN
GRDBEN
BUFEN
U14
U14
+5V
R18
IO
U21

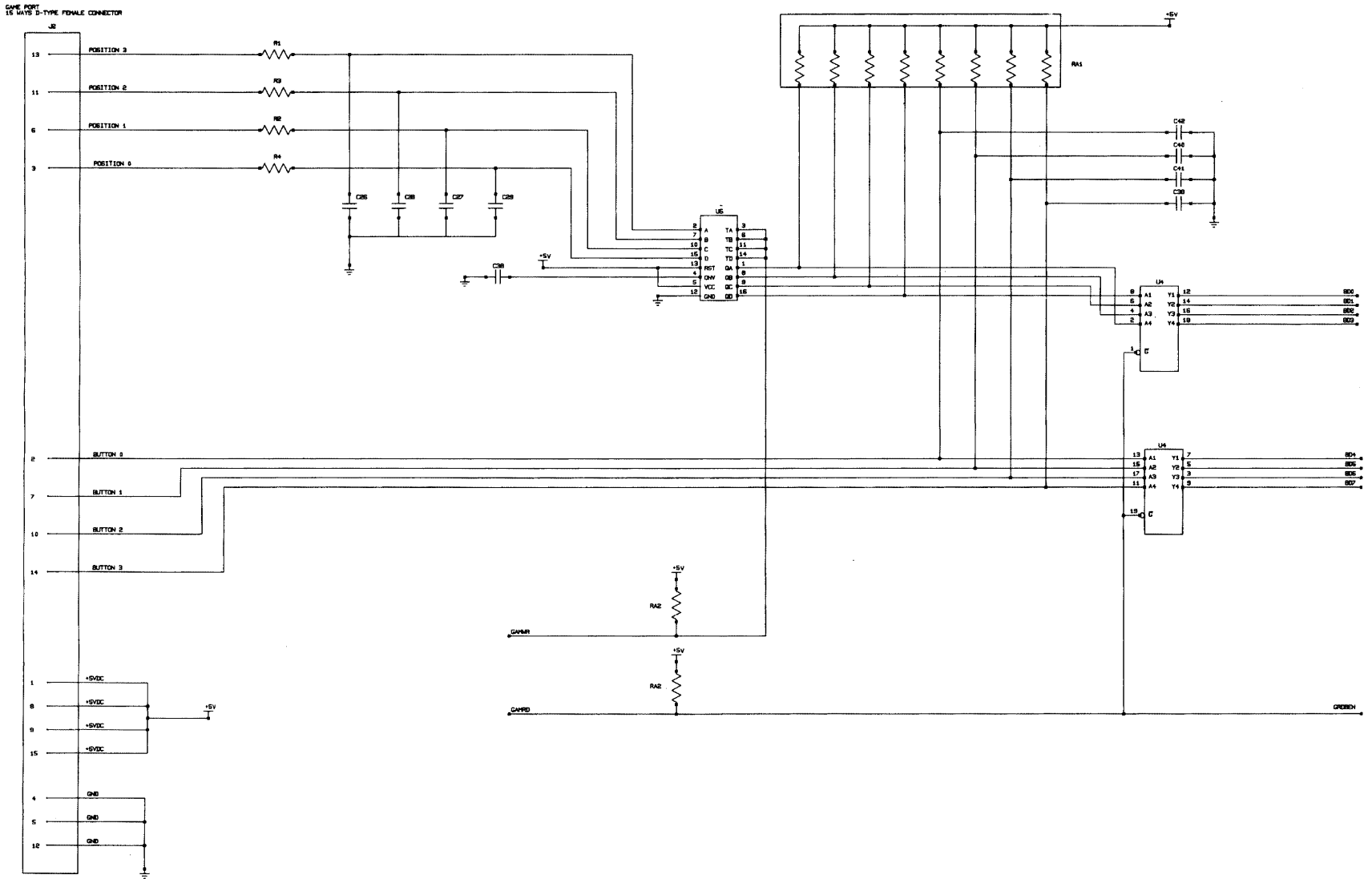

STROBE
AUTOFD
INIT
SLCTIN
WRPTL
BAEN
BIOR
BIOW
BA0
BA1
BA2
BA3
BA4
BA5
BA6
BA7
BA8
BA9
BA10
PTL0
PTL1
PTL2
PTL3
PTL4
PTL5
PTL6
PTL7
BUFEN
EXSTB
EXAUFD
EXINIT
EXSLCT
SLCT
PE
ACK
BUSY
GAMRD
GAMWR
RST
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BD0
INDEX
ERROR
IRQ7
RAMDA
FDDRQ
FDDACK
FDMDA
FDME1
SEPCLK
SEPDA
DMOUT
SEDOUT
TC
FDPS1
FDPS0
IRQGT
IRQOUT
U69
C1
+5V
L48
C79
XTAL1
U13
R7
R8
C82
C81
C80
XTAL2
R9
R10
C84

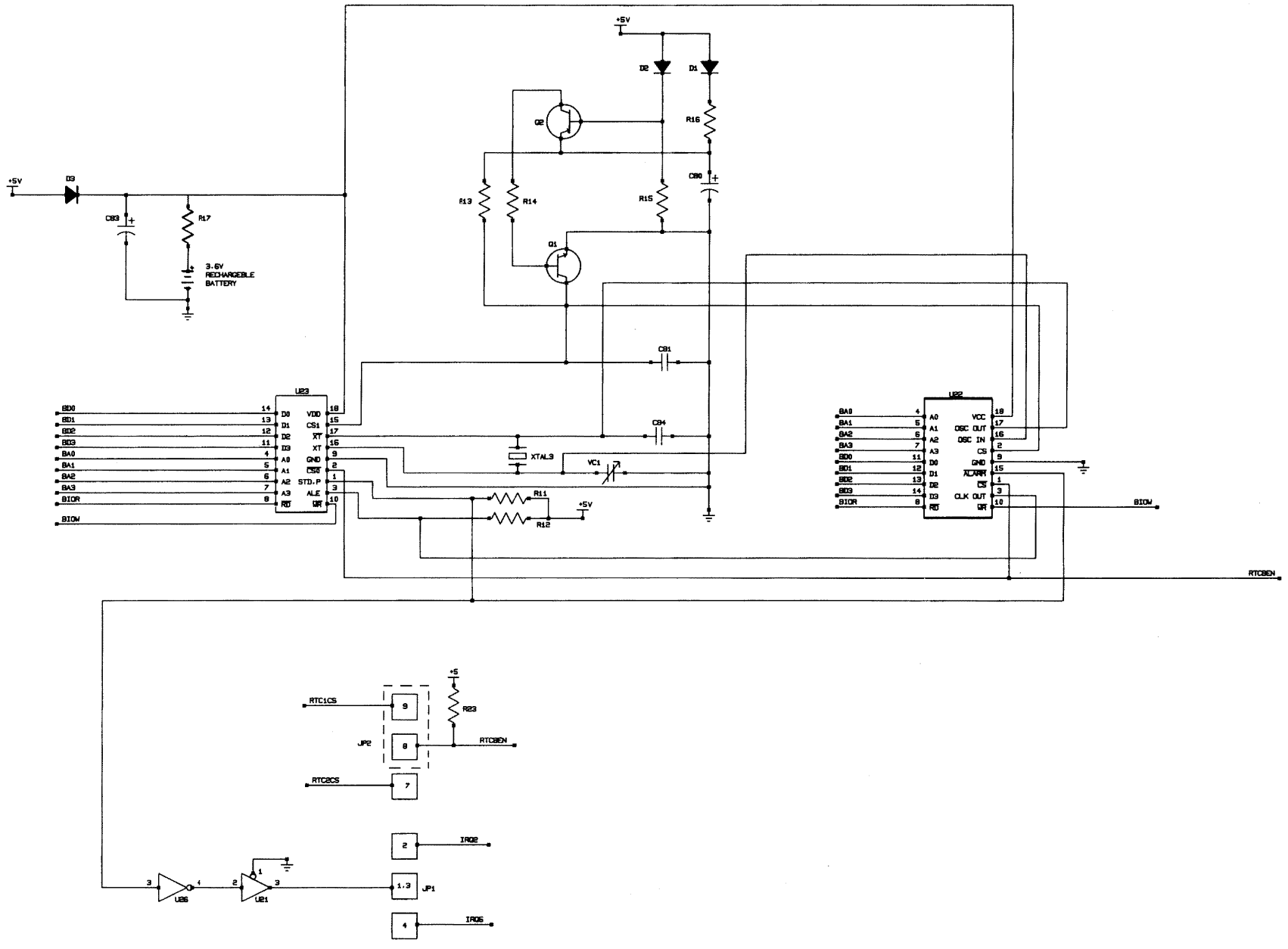

+5V
TCEN0
ENABLE
DISABLE
JP2
TCABEL2
TCABEL1
FDEN0
DISABLE
ENABLE
DRQOUT
DRQIN
U41
RESET
RD
WR
CS
A0
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DRQ
DACK
TC
IDX
INT
CLK
VCC
RW/SEEK
LCT/DIR
FR/CTP
HDL
RDY
WP/TS
FLT/TRK0
PS0
PS1
WDA
WG
WE
VCC
RD
RDW
WCK
GND
FDRES
FDCRD
FDCWR
DA1
DA0
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
FDDRQ
FDDACK
FDCTC
F4M
IRQ6
FDPS0
FDPS1
FDWDA
FDWE1
FDWRCK
DMAGT
N.C.
U26
U27
U28
U29
U30
U31
U32
U33
U34
U35
U36
U37
U38
U39
U40
GDSEL2
GDSEL1
CLD4
CLD5
DME
DMDA
RAWDA
INDEX
SEPDA
SEPCLK
SEPDOUT
DMOUT
JP3
JP4
R19
R22
R20
R21
J5
FLOPPY DISK DRIVE CONNECTOR
DRIVE SEL2
DRIVE SEL1
MOTOR EN1
MOTOR EN2
WRITE ENABLE
STEP
DIRECTION
SELECT HEAD 1
WRITE DATA
TRACK0
WRITE PORT
INDEX
READ DATA
2,4,6,34
1,3,5.....33
(ODD PINS)
21,22.....37
PINS
U24
VCC
INRQ
SEPDT
CD1
SEPCK
CD0
RCLK
(NORMALLY NOT USE)

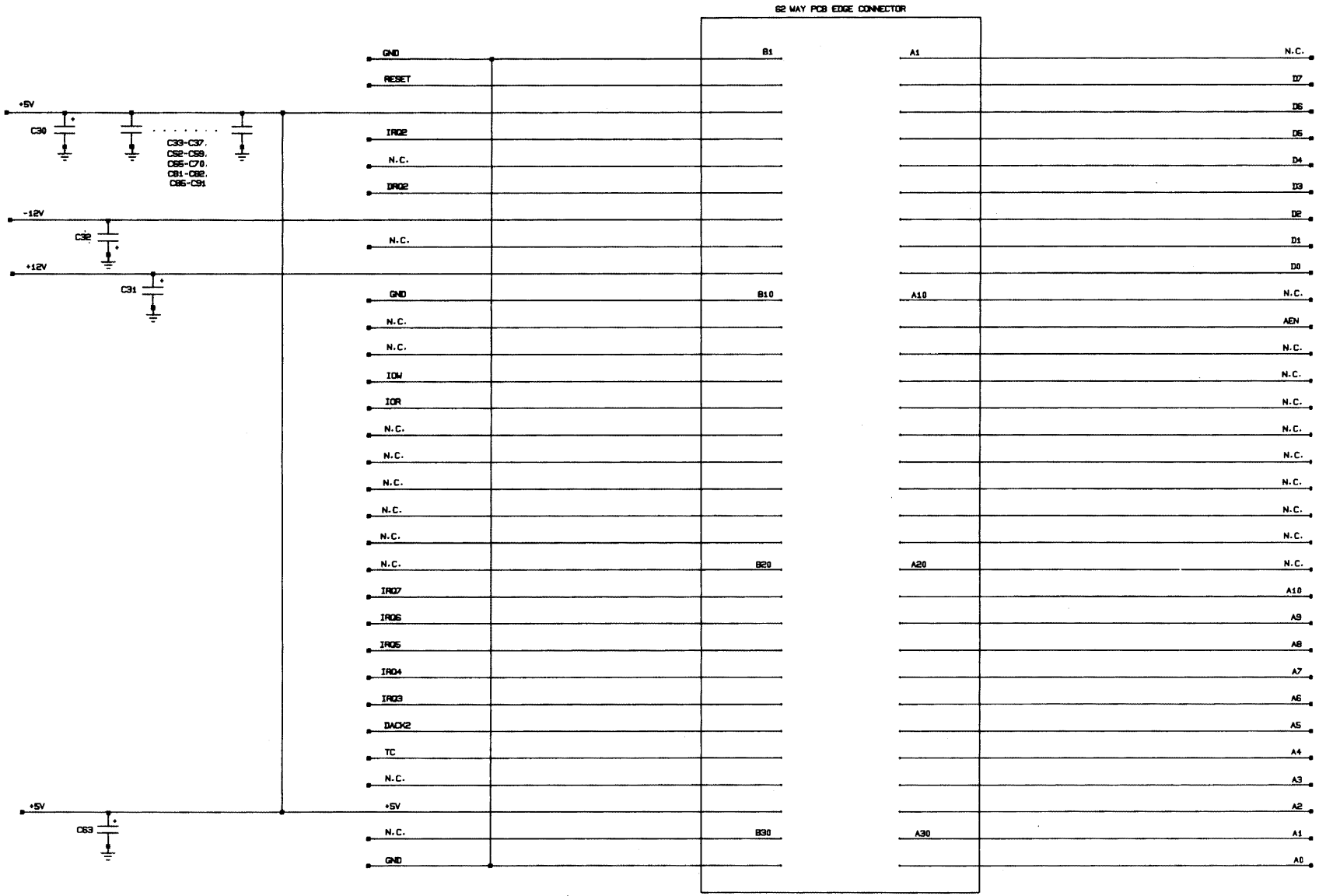

PRINTER PORT CONNECTOR
STROBE
AUTOFD
INIT
SLCTIN
ERROR
PTRDIS
PTABEL
ENABLE
DISABLE
JPR

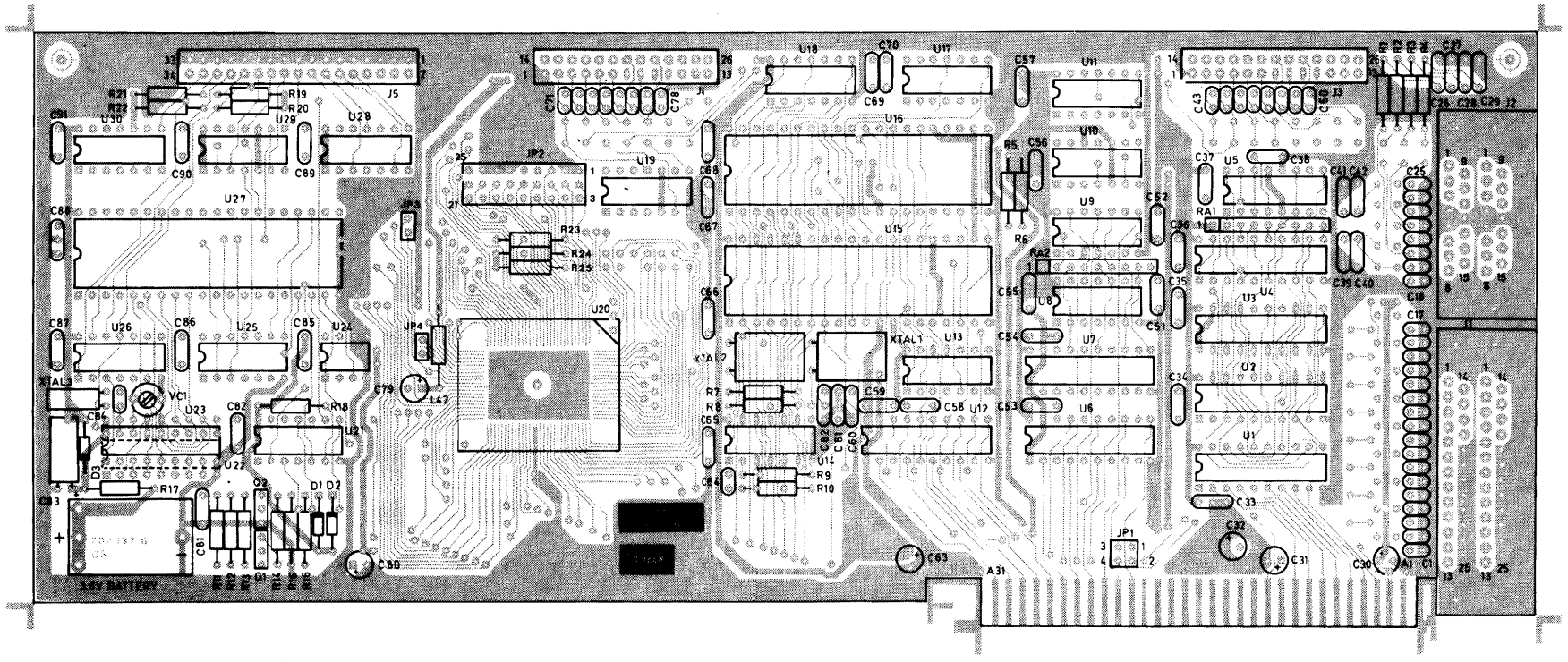

SERIAL PORT COM 1
DB9 MALE
CONNECTOR
COM PORT HEADER
J3
TX
RX
RTS
CTS
DTR
DSR
RTSD
RI
GND
GND
U16
JP2
DISABLE
ENABLE
COM1CS
FIMB
COM1BN
BIOW
RP4
RP6
RA2
U10
U9
U11
U17
RST
BA0
BA1
BA2
BIOR
IRQ4
N.C.
+5V
+12V
-12V

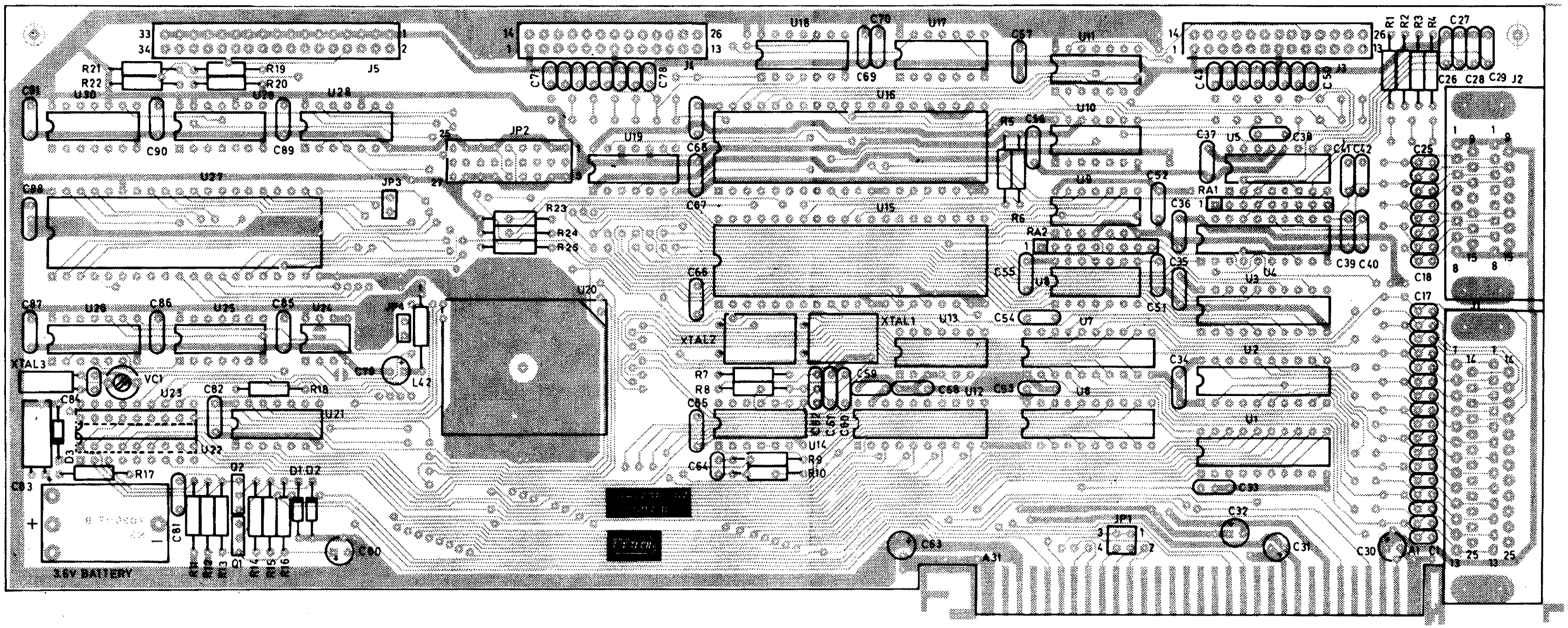

SERIAL PORT COM2
DB9 MALE CONNECTOR
COM PORT HEADER
J4
TX
RX
RTS
CTS
DTR
DSR
RLSD
RI
GND
GND
U15
D0
D1
D2
D3
D4
D5
D6
D7
RCLK
SIN
SOUT
CS0
CS1
CS2
BAUDOUT
XTAL1
XTAL2
DOSTR
DOSTR
GND
VCC
RI
RLSD
DSR
CTS
MR
OUT1
DTR
RTS
OUT2
INTRPT
NC
A0
A1
A2
ADS
CSOUT
DDIS
DISTR
DISTR
+5V
JP2
DISABLED
ENABLED
COM2CS
FIN8
COM8EN
8IOW
R25
R5
RA2
N.C.
RESET
12V
-12V
BA0
BA1
BA2
8IOR
IRQ8
U16
U17
U18
U19


GAME PORT
15 WAYS D-TYPE FEMALE CONNECTOR
J2
POSITION 3
POSITION 2
POSITION 1
POSITION 0
R1
R3
R2
R4
C25
C26
C27
C28
C30
U5
RA1
C42
C40
C41
C39
U4
BD0
BD1
BD2
BD3
BUTTON 0
BUTTON 1
BUTTON 2
BUTTON 3
+5VDC
GND
RA2
GAMBR
GAMBD
GREEN


+5V
D3
CB3
R17
3.6V
RECHARGEBLE
BATTERY
D2
D1
Q2
R16
CB0
R13
R14
R15
Q1
CB1
CB4
XTAL3
VC1
R11
R12
+5V
U23
BD0
BD1
BD2
BD3
BA0
BA1
BA2
BA3
BIOR
BIOW
D0
D1
D2
D3
A0
A1
A2
A3
RD
VDD
CS1
XT
XT
GND
CS0
STD.P
ALE
WR
U22
BA0
BA1
BA2
BA3
BD0
BD1
BD2
BD3
BIOR
A0
A1
A2
A3
D0
D1
D2
D3
RD
VCC
OSC OUT
OSC IN
CS
GND
ALARM
CS
CLK OUT
WR
BIOW
RTCBEN
RTC1CS
JP2
R23
RTCBEN
RTC2CS
IRQ2
JP1
IRQ6
U86
U21


62 WAY PCB EDGE CONNECTOR
+5V
C30
C33-C37,
C52-C59,
C65-C70,
C81-C82,
C85-C91
-12V
C32
+12V
C31
+5V
C63
GND
RESET
IRQ2
N.C.
DRQ2
N.C.
GND
N.C.
N.C.
IOW
IOR
N.C.
N.C.
N.C.
N.C.
N.C.
N.C.
IRQ7
IRQ6
IRQ5
IRQ4
IRQ3
DACK2
TC
N.C.
+5V
N.C.
GND
B1
B10
B20
B30
A1
A10
A20
A30
N.C.
D7
D6
D5
D4
D3
D2
D1
D0
N.C.
AEN
N.C.
N.C.
N.C.
N.C.
N.C.
N.C.
N.C.
N.C.
N.C.
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0


J5
J4
J3
J2
J1
JP1
JP2
JP3
JP4
U30
U29
U28
U27
U26
U25
U24
U23
U22
U21
U20
U19
U18
U17
U16
U15
U14
U13
U12
U11
U10
U9
U8
U7
U6
U5
U4
U3
U2
U1
XTAL1
XTAL2
VC1
L42
A31
3.6V BATTERY


J5
R21
R22
R19
R20
C91
U30
U29
U28
C90
C89
JP2
U19
U18
U17
C70
C69
C71
C78
J4
U16
U11
U10
C57
J3
C43
C50
R1
R2
R3
R4
C27
C26
C28
C29
J2
C88
U27
JP3
R23
R24
R25
C65
C67
U15
R5
R6
C56
U9
C37
U5
C38
C41
C42
C52
RA1
C36
RA2
C25
C18
C87
U26
C86
U25
C85
U24
JP4
U20
C66
C55
U8
C35
U3
U4
C39
C40
C17
XTAL3
VC1
C79
L42
XTAL2
XTAL1
U13
C54
U7
C51
U2
C34
C84
U23
C82
R18
U21
U22
R7
R8
C85
C59
C60
U12
C53
U6
U14
U1
C64
R9
R10
C83
R17
Q2
D1
D2
C81
Q1
3.6V BATTERY
C80
C63
A31
JP1
C32
C31
C30
C33
A1

LASER MULTI-I/O CARD (G/A) COMPONENT LOCATION LIST

DESTINATION	PART NUMBER	DESCRIPTION
J2	40-0388-15-02	D15 FEMALE CONNECTOR(PCB TYPE)
J1	40-0388-25-02	D25 FEMALE CONNECTOR(PCB TYPE)
JP1	40-0184-00-01	WAFER 2 PINS (CPI)
	v40-0184-00-00	WAFER 2 PINS (MOLEX)
JP2	40-0215-00-01	WAFER 3 PINS (CPI)
	v40-0215-00-00	WAFER 3 PINS (MOLEX)
J3,J4	40-0194-00-01	WAFER 13 PINS (CPI)
	v40-0194-00-00	WAFER 13 PINS (MOLEX)
J5	40-0194-00-01	WAFER 13 PINS (CPI)
	v40-0194-00-00	WAFER 13 PINS (MOLEX)
AND	40-0216-00-01	WAFER 4 PINS (CPI)
	v40-0216-00-00	WAFER 4 PINS (MOLEX)
U20	27-0604-00-00	GATE ARRAY C1
U18	40-0283-01-01	I.C. SOCKET 14 PINS (FOR 1488)
U19	40-0283-01-01	I.C. SOCKET 14 PINS (FOR 1489)
U27	27-0525-00-02	I.C. FDC (ZILOG) Z765A08PSC
	v27-0525-00-00	I.C. FDC (NEC) UPD765AC
	v27-0525-00-01	I.C. FDC (ROCKWELL) UPD765A
U16	27-0365-00-00	I.C. IN8250 (N.S.)
	v27-0365-00-01	I.C. WD8250 (WESTERN)
U15	40-0008-00-03	I.C. SOCKET 40 PINS FOR IN8250
	v40-0008-00-00	I.C. SOCKET 40 PINS FOR IN8250
U23	27-0619-01-00	RTC MSM6242BRS (OKI)
	a27-0619-00-00	RTC MSM6242RS (OKI)
OR	27-0498-00-00	RP5C15 (USE U22 LOCATION)
U5	27-0201-00-02	QUAD TIMER XR-558 (EXAR)
	v27-0201-00-01	I.C. NE558 (SIGNETICS)
U10	27-0363-00-05	XR1488 (EXAR)
	v27-0363-00-00	MC1488 (MOTOROLA)
	v27-0363-00-01	MC1488 (TEXAS)
	v27-0363-00-02	MC1488 (SIGNETICS)
U11,U17	27-0364-00-05	XR1489 (EXAR)
	v27-0364-00-00	MC1489 (MOTOROLA)
	v27-0364-00-02	MC1489 (SIGNETICS)
U2	27-0195-00-00	I.C. 74LS374 (MOTOROLA)
	v27-0195-00-01	I.C. 74LS374 (T.I.)
	v27-0195-00-02	I.C. 74LS374 (HITACHI)
	v27-0195-00-03	I.C. 74LS374 (FAIRCHILD)
U1	27-0100-00-01	I.C. 74LS245 (MOTOROLA)
	v27-0100-00-02	I.C. 74LS245 (FAIRCHILD)
	v27-0100-00-03	I.C. 74LS245 (HITACHI)
	v27-0100-00-04	I.C. 74LS245 (T.I.)
	v27-0100-00-05	I.C. 74LS245 (MITSUSIDER)
	v27-0100-00-06	I.C. 74LS245 (MATSUSHITA)
	v27-0100-00-07	I.C. 74LS245 (N.S.)

U3,U4,U6,	27-0160-00-00	I.C. 74LS244 (MOTOROLA)
U7,U12	v27-0160-00-01	I.C. 74LS244 (FAIRCHILD)
	v27-0160-00-02	I.C. 74LS244 (HITACHI)
	v27-0160-00-03	I.C. 74LS244 (T.I.)
	v27-0160-00-04	I.C. 74LS244
	v27-0160-00-05	I.C. 74LS244 (MATSUSHITA)
	v27-0160-00-06	I.C. 74LS244 (N.S.)
	v27-0160-00-07	I.C. 74LS244 (SGS)
U14,U26	27-0038-02-00	I.C. 74LS04 (HITACHI)
	v27-0038-02-01	I.C. 74LS04 (SCISYS)
	v27-0038-02-02	I.C. 74LS04 (FAIRCHILD)
	v27-0038-02-03	I.C. 74LS04 (MOTOROLA)
	v27-0038-02-04	I.C. 74LS04 (N.S.)
	v27-0038-02-05	I.C. 74LS04
	v27-0038-02-06	I.C. 74LS04 (SGS)
	27-0057-00-02	I.C. 74LS05 (HITACHI)
	v27-0057-00-03	I.C. 74LS05 (TEXAS)
	v27-0057-00-01	I.C. 74LS05 (SCISYS)
	v27-0057-00-04	I.C. 74LS05 (N.S.)
	v27-0057-00-05	I.C. 74LS05 (MOTOROLA)
U25	27-0184-00-00	I.C. 74LS08 (HITACHI)
	v27-0184-00-01	I.C. 74LS08
	v27-0184-00-04	I.C. 74LS08 (TEXAS)
	v27-0184-00-05	I.C. 74LS08 (MOTOROLA)
	a27-0444-00-00	I.C. 74HCT08 (RCA)
U9,U21	27-0209-00-01	I.C. 74LS125 (HITACHI)
	v27-0209-00-00	I.C. 74LS125 (MOTOROLA)
	v27-0209-00-03	I.C. 74LS125 (TEXAS)
U13	27-0171-00-04	I.C. 74LS30 (HITACHI)
	v27-0171-00-00	I.C. 74LS30 (MOTOROLA)
	v27-0171-00-01	I.C. 74LS30 (FAIRCHILD)
	v27-0171-00-03	I.C. 74LS30 (TEXAS)
U28,U29,U30	27-0241-00-01	I.C. 7438 (TEXAS)
	v27-0241-00-00	I.C. 7438 (MOTOROLA)
RA1,RA2	26-1472-08-13	RESISTOR NETWORK 4K7x8,9 PINS
	v26-1472-08-00	RESISTOR NETWORK 4K7x8,9 PINS
	v26-1472-08-01	RESISTOR NETWORK 4K7x8,9 PINS
	v26-1472-08-02	RESISTOR NETWORK 4K7x8,9 PINS
	v26-1472-08-05	RESISTOR NETWORK 4K7x8,9 PINS
XTAL2	25-3026-00-03	CRYSTAL 16MHZ (IPL)
	v25-3026-00-00	CRYSTAL 16MHZ (NAKAGAWA)
XTAL3	25-3009-00-03	CRYSTAL 32.768KHZ (IPL)
	v25-3009-00-00	CRYSTAL 32.768KHZ (DAIWA)
	a25-3009-01-03	CRYSTAL 32.768KHZ (DAIWA)
XTAL1	25-3045-01-00	CRYSTAL 3.6864MHZ (SUNNY)
	a25-3045-00-00	CRYSTAL 3.6864MHZ (DAIWA)
L42	25-1022-01-00	CHOKE COIL 1mH, +/-5% (TDK)
	a25-1022-00-00	CHOKE COIL 1mH, +/-10% (TDK)
R7-R10,R17	23-0013-10-02	RESISTOR 1K OHM +/-5% 1/4W
	v23-0013-10-00	RESISTOR 1K OHM +/-5% 1/4W
R19-R22	23-0151-10-02	RESISTOR 150 OHM +/-5% 1/4W
	v23-0151-10-00	RESISTOR 150 OHM +/-5% 1/4W
R13-R15	23-0333-10-02	RESISTOR 33K OHM +/-5% 1/4W
	v23-0333-10-00	RESISTOR 33K OHM +/-5% 1/4W

R5,R6,R18,	23-0472-10-02	RESISTOR 4K7 OHM +/-5% 1/4W
R16,R11,R12,	v23-0472-10-00	RESISTOR 4K7 OHM +/-5% 1/4W
R23-R25		
R1-R4	23-0222-10-02	RESISTOR 2K2 OHM +/-5% 1/4W
	v23-0222-10-00	RESISTOR 2K2 OHM +/-5% 1/4W
	a23-0222-16-00	RESISTOR 2K2 OHM +/-5% 1/16W
	a23-0222-16-01	RESISTOR 2K2 OHM +/-5% 1/16W
C30-C32,C63,	22-1100-21-03	ELEC CAP 10UF 16V +/-20%
C79,C80,C83	v22-1100-21-00	ELEC CAP 10UF +/-20% 16V
C38	22-3103-28-00	CER CAP 0.01UF +80 -20% 50V
	v22-3103-28-02	CER CAP 0.01UF +80 -20% 50V
	v22-3103-28-15	CER CAP 0.01UF +80 -20% 50V
C33-C37,	22-3104-28-33	MONO CAP 0.1UF +80 -20% 50V
C52,C59,	v22-3104-28-37	MONO CAP 0.1UF +80 -20% 50V
C65-C70,	v22-3104-28-40	MONO CAP 0.1UF +80 -20% 50V
C85-C91,	v22-3104-28-53	MONO CAP 0.1UF +80 -20% 50V
C81,C82	v22-3104-28-67	MONO CAP 0.1UF +80 -20% 50V
	v22-3104-28-68	MONO CAP 0.1UF +80 -20% 50V
C64,C39-C42	22-3470-26-00	CER CAP 47PF +/-10% 50V
C62	22-3221-26-00	CER CAP 220PF +/-10% 50V
C61	22-3271-26-00	CER CAP 270PF +/-10% 50V
C60	22-3331-26-00	CER CAP 330PF +/-10% 50V
C5-C12	22-3222-28-00	CER CAP 0.0022UF -20% 50V
C26-C29	22-6103-26-01	MYLAR CAP 0.01UF +/-10% 50V
	v22-6103-26-11	MYLAR CAP 0.01UF +/-10% 50V
	a22-6103-46-40	MYLAR CAP 0.01UF +/10% 100V
VC1	22-7002-01-00	TRIMMER CAP 20PF
	a22-7002-00-00	TRIMMER CAP 20PF
D1-D3	21-0001-00-00	DIODE IN4148 (FAIRCHILD)
	a21-0008-00-00	DIODE IN914 (FAIRCHILD)
	a21-0001-00-01	DIODE IN4148 (NEC)
	a21-0001-00-02	DIODE IN4148 (PHILIPS)
	a21-0001-00-03	DIODE IN4148
Q2	20-0025-03-00	TRANSISTOR 1402D (PHILIPS)
	a20-0041-00-01	TRANSISTOR 2N3904 (FAIRCHILD)
	a20-0041-00-00	TRANSISTOR 2N3904 (MOTOROLA)
	v20-0025-03-01	TRANSISTOR ST 1402D (SIEMENS)
	v20-0025-03-02	TRANSISTOR 1402D (PHILIPS)
Q1	20-0039-00-02	TRANSISTOR 2N3906 (FAIRCHILD)
	v20-0039-00-01	TRANSISTOR 2N3906 (MOTOROLA)

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